

Failure Mechanism and Reinforcement Technology of 55 nm CMOS Inverter Induced by High-power Microwave

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High-power electromagnetic pulses can transmit a large induced electromotive force or energy through metal interconnection lines, causing interference or damage to integrated circuits. CMOS circuits are the basic components of sensors, so sensors that work in an electromagnetic environment may malfunction. It is of great importance to study the anti-electromagnetic damage technology of CMOS inverters. On the basis of the simulation using Sentaurus, an electrothermal coupling model of a 55 nm CMOS inverter is established. The simulation results show that the latch-up effect is the main mechanism of CMOS failure. In view of the failure process under different high-power microwave (HPM) pulse parameters, we propose a CMOS inverter reinforcement technology. Research shows that the source injection current of the reinforced structure is more than ten times less than that of the traditional structure under electromagnetic interference, which effectively suppresses the occurrence of latch-up.

1. Introduction

In 1962, electromagnetic pulse effects were first observed in the United States during high-altitude nuclear explosions.⁽¹⁾ High-power microwave (HPM) is a form of intense electromagnetic pulse characterized by high frequency and power. Electronic systems are extremely sensitive to external electromagnetic energy. A sensor is the primary link for electronic systems to realize automatic detection and automatic control. The conversion and driver circuits in the sensor are based on MOSFETs. When a high-power electromagnetic pulse is coupled into the integrated circuit through the antenna or circuit pins, it will cause temporary upset, permanent upset or permanent physical damage to the entire system.⁽²⁾ Therefore, the engineering protection theory and reliability technology of the electromagnetic pulse have become research hotspots in various countries around the world.^(3–5)

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At present, some important research results on the mechanism of HPM pulse damage to CMOS inverters have been reported. Hwang *et al.* studied the delay time and breakdown effects of high-power microwaves on CMOS inverters.⁽⁶⁾ Chen and Du proposed a semi-empirical theoretical model based on simulation results, which was used to quantitatively analyze the impact of pulse width and frequency on the latch-up effect.⁽⁷⁾ Yu *et al.* studied the temperature dependence of the latch-up effects in a CMOS inverter based on the 0.5 μm technology caused by a high-power microwave.⁽⁸⁾ Holloway *et al.* simulated the influence of power supply voltage on the electromagnetic pulse damage effect of CMOS inverters.⁽⁹⁾ However, they did not study the anti-electromagnetic reinforcement technology of CMOS inverters based on the damage mechanism.

In this paper, the peak temperature and current change curves of a CMOS inverter under the influence of different HPM pulses are analyzed, aiming to facilitate the understanding of the latch-up mechanism. In consideration of the failure mechanism, a reinforced structure of the CMOS inverter is proposed.

2. Test Structure and Model

2.1 Device model

The CMOS inverter is constructed on the basis of 55 nm CMOS technology. The lateral device size (x -axis) and depth (y -axis) are 3 and 1.5 μm , respectively. The power supply voltage is chosen as 1.5 V. Owing to the selection of the N-well process, the substrate is p-type-doped and the N-well is generated by diffusion. The N-channel and P-channel MOSFETs are respectively fabricated on the P-substrate and N-well. The source and drain regions are formed by ion implantation. As shown in Fig. 1, the inverter made by this process will have two parasitic transistors, Q_1 and Q_2 , as well as the substrate resistance R_S and well resistance R_W .

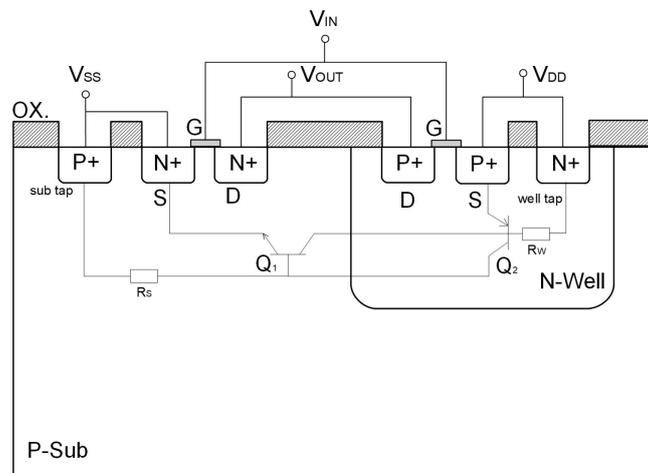


Fig. 1. Basic schematic of CMOS inverter.

2.2 Simulation circuit

Generally speaking, HPM radiated energy is coupled to the internal electronic equipment of the system through the front-door or back-door path.⁽¹⁰⁾ In this investigation, the HPM is assumed to be a sinusoidal plane wave without attenuation⁽¹¹⁾ and is injected into the “S” contact of the N-channel MOSFET to simulate the situation that the HPM pulse couples into the CMOS inverter through the back-door path. To accurately simulate the response behavior of the CMOS inverter to the HPM pulse, a 100 Ω load resistor is connected in series between the excitation signal and the “S” contact. A constant ambient temperature (300 K) is set at the bottom side of the CMOS inverter. The power supply voltage VDD is set to 1.5 V. The schematic of the electromagnetic damage effect simulation circuit is shown in Fig. 2.

2.3 Physical model

The P-substrate/n+ source junction is triggered into forward bias during the negative half-period of the sinusoidal voltage. A large number of electrons in the source region are injected into the p-type substrate. A certain proportion of the electrons will be recombined, and the other part of the electrons are collected by the N-well. This process will produce the corresponding currents I_{sub} and I_{well} .⁽¹²⁾ The current flows through R_S and R_W will produce a voltage drop. If this voltage drop is sufficiently large, the parasitic transistors Q_1 and Q_2 will turn on. When the product of the common base current gains of the parasitic transistors Q_1 and Q_2 exceeds 1, the positive feedback between the two parasitic transistors will continue. A large current path will be generated from the power supply (VDD) trail to the ground (GND), and a latch-up effect will occur. The static power consumption of the CMOS inverter during normal operation is very low, but the latch-up effect will rapidly increase the power consumption of the circuit. At the same time, the heat accumulation inside the circuit will eventually cause the circuit to be damaged or burned. A large number of studies have revealed that the latch-up effect is the main cause of electromagnetic damage to CMOS inverters.^(13–15)

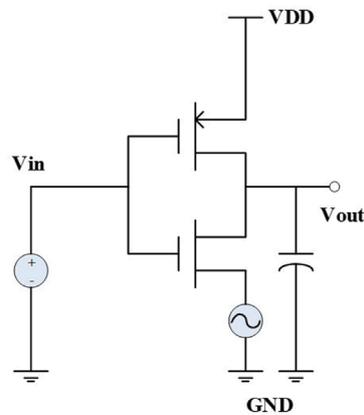


Fig. 2. (Color online) Schematic of simulation circuit.

Under the influence of HPM, the environmental electric field intensity of the CMOS inverter is usually very high. Owing to the scattering of ionized impurities, the carrier drift velocity is no longer proportional to the electric field intensity, but close to saturation. Therefore, a high-field saturation model (Canali model) is adopted and revised as follows:

$$\mu(F) = \frac{\mu_{low}}{\left[1 + \left(\frac{\mu_{low}}{v_{sat}}\right)^\beta\right]^{\frac{1}{\beta}}}. \quad (1)$$

Here, v_{sat} is the saturation value of the carrier drift velocity, and the parameter β is related to temperature as follows:

$$\beta = \left(\frac{T}{T_0}\right)^{\beta^{exp}}. \quad (2)$$

The values of the parameters β and β^{exp} in the Si material are shown in Table 1.

To solve the problem of the CMOS inverter response to HPM, both the current density distribution and the thermal field distribution must be considered. It is necessary to solve the coupling of the electric field and thermal field.

3. Numerical Simulation

The input signal V_{in} is a periodic square wave with a period of 20 ns, a voltage amplitude of 1.5 V, and a duty cycle of 50%, and the HPM pulse is a sinusoidal signal with a frequency of 1 GHz and a pulse width of 10 ns. As shown in Fig. 3, the transient characteristic curve was obtained by changing the voltage amplitude of HPM pulses at the “S” contact of the N-channel MOSFET.

It can be seen from Fig. 3(a) that when there is no HPM pulse injection (source InnerVoltage is 0 V), the function of the CMOS inverter is normal. When an HPM pulse with a voltage amplitude of 1 V is on, the output of the CMOS inverter malfunctions within 10 ns, but returns to normal function as soon as the HPM pulse is removed. After the voltage amplitude of the HPM pulse is increased to 1.2 V, the output of the CMOS inverter is also abnormal during the pulse width time. However, the output voltage of the CMOS inverter does not return to normal but stays at around 1.3 V after the HPM pulse is removed, indicating that a malfunction has appeared. The 1.2 V input voltage has reached the damage voltage threshold of the CMOS inverter.

Table 1
High electric field saturation model parameters in Si material.

Parameter	Electron	Hole
β	1.109	1.213
β^{exp}	0.66	0.17

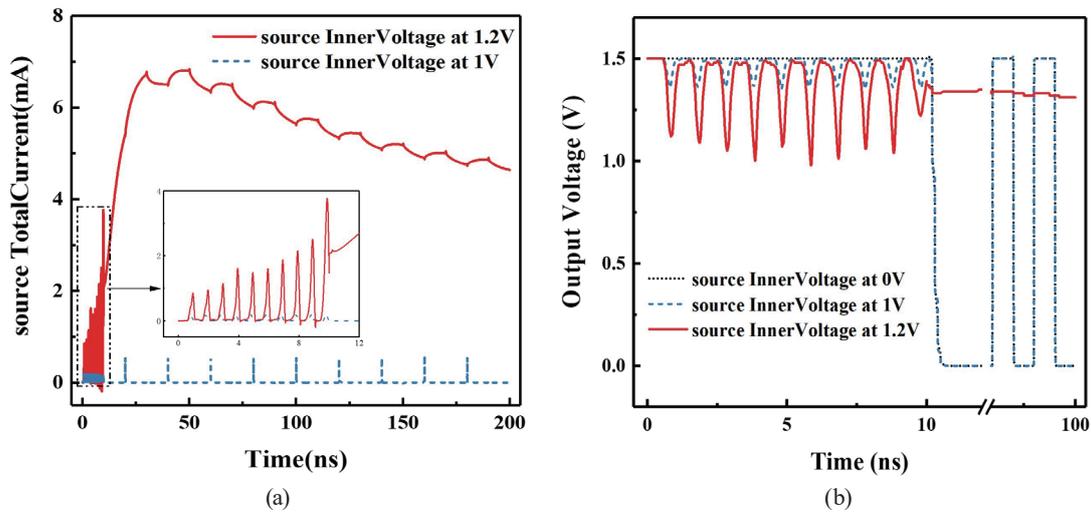


Fig. 3. (Color online) (a) Responses of CMOS inverter without HPM and with HPM at 1 and 1.2 V. (b) Variation of source current versus time in two cases.

From the previous discussion, it can be considered that the main failure mechanism of the CMOS inverter is the latch-up effect, which leads to a high current path between VDD and GND. To visualize the effect, the power supply current curves of the CMOS inverter in two cases are depicted in Fig. 3(b). When an HPM pulse with a voltage amplitude of 1 V is exerted, the power supply current remains below 200 μ A. After the HPM is no longer active, the supply current returns to zero. When the voltage amplitude of the HPM pulse is increased to 1.2 V, the power current of the CMOS inverter changes periodically within 10 ns. After the HPM pulse is removed, the power current firstly increases and then decreases, reaching a peak of about 6.8 mA. Therefore, the latch-up effect of the CMOS inverter has occurred under the influence of the HPM pulse with this amplitude. A large current path between VDD and GND causes the device temperature to increase.

The boundary condition of temperature was selected as 300 K in the modeling of the CMOS inverter. Owing to the thermal effect of the HPM pulse, the internal temperature of the CMOS inverter will increase under the action of the HPM pulse. Figure 4 shows the internal temperature change curves of the CMOS inverter under different HPM voltage amplitudes. When the voltage amplitude of the HPM pulse is 1 V, the peak temperature changes periodically within 10 ns. The maximum temperature reaches 304 $^{\circ}$ C, and the temperature basically stays at 301 $^{\circ}$ C after the HPM pulse is removed. When the voltage amplitude of the HPM pulse is increased to 1.2 V, the peak temperature increases to 313 $^{\circ}$ C within 10 ns. After the HPM is removed, the maximum temperature decreases at first and then increases again continuously.

As Fig. 4 shows, the temperature increases during the negative half-period of the pulse but decreases slightly upon the occurrence of the positive half-period. To verify this rule, two time nodes, 7.95 and 8.45 ns, were selected to measure the current density distribution inside the CMOS inverter (depicted in Fig. 5). The current density at 7.95 ns is significantly higher than at 8.45 ns. Upon the occurrence of the negative half-period (at 7.95 ns), the P-substrate/ n^+ source

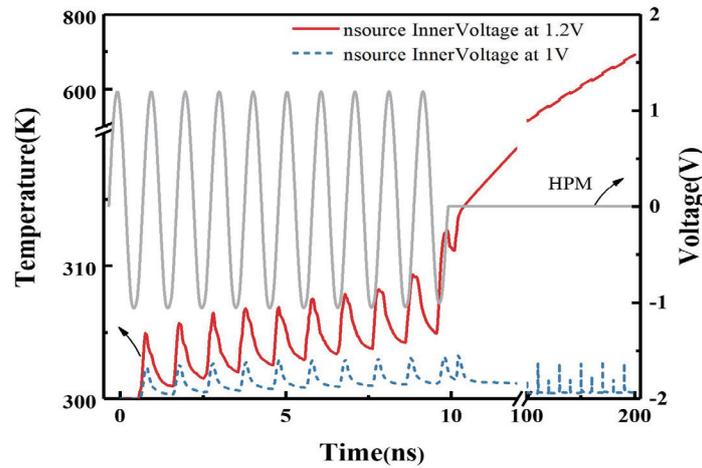


Fig. 4. (Color online) Variation of maximum temperature in CMOS inverter versus time in two cases.

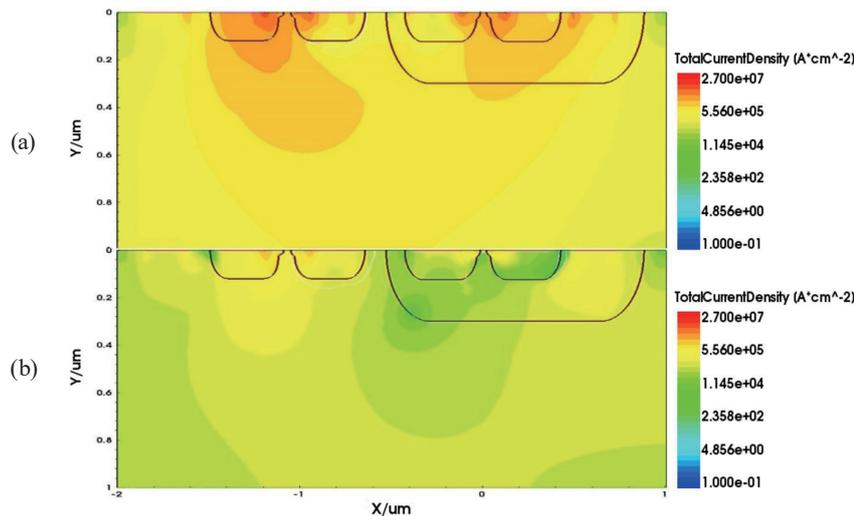


Fig. 5. (Color online) Current density distribution in CMOS inverter at (a) 7.91 ns and (b) 8.42 ns.

junction becomes a forward bias. Then the current path from the P-substrate contact to the n^+ source contact forms, which leads to the temperature increase. At 8.45 ns, the P-substrate/ n^+ source junction becomes a reverse bias, the current path from the P-substrate contact to the n^+ source contact does not form, and hence the temperature decreases.

Because of the temperature variation of the CMOS inverter under the influence of HPM, heat accumulation and the latch-up effect may lead to thermal burning of the device. Figure 6 shows that when the voltage amplitude of the HPM pulse is 6 V, the peak temperature at 522 ns will increase to 1688 K due to the latch-up, reaching the melting point of the silicon material. When the voltage amplitude of the HPM pulse is increased to 9.5 V, the device will be burned due to heat accumulation at the 12th cycle of the pulse. As the voltage amplitude of the HPM pulse continues to increase to 14 V, the device will be destroyed during the first cycle of the HPM pulse.

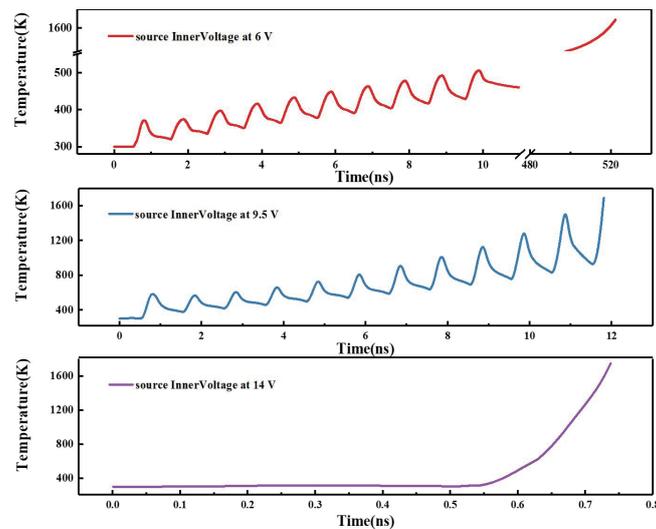


Fig. 6. (Color online) Peak temperature change of CMOS inverter with different HPM pulse amplitudes.

Simulation results show that when the number of electrons injected into the substrate is sufficient to maintain the positive feedback between the two parasitic transistors, the thermal effect generated by the large current will destroy the device. Referring to the positive feedback mechanism of latch-up effect, we found that the latch resistance can be effectively improved by decoupling two parasitic transistors. Therefore, conventional CMOS inverter reinforcement schemes reduce the current gain by increasing the base width of the transverse parasitic triode, or reduce the equivalent resistances R_S and R_W by introducing protection ring technology in the layout design. In this study, the reinforcement technology can not only reduce the influence of parasitic parameters (such as the P-substrate resistance R_S and the N-well resistance R_W), but also avoid the electron injection into the substrate during the negative half-cycle of the HPM pulse. The latch-up effect is suppressed without adding additional process steps.

The cross section of the reinforced CMOS inverter is shown in Fig. 7. The source and drain regions of the N-channel MOSFET are switched in their spatial location and connection relationship. A p-type active region is formed adjacent to the source region, and the two regions are connected by interconnecting metal wires. In this structure, the source region of the N-channel MOSFET reaches the newly added p-type active region through an ohmic contact, and then the substrate and the substrate contact. The shunt resistance R_S between the base and emitter of the parasitic NPN transistor will be absent, eliminating its influence on the latch-up effect. At the same time, the N-channel MOSFET source region forms an ohmic contact with the p-type active region through interconnecting metal wires. When an HPM pulse is injected into the source region, the p-type active region will also be injected. The voltage drop across the P-substrate/ n^+ source junction is reduced, which inhibits the electron injection into the substrate. The reduction in the number of electrons will suppress the latch-up effect.

As depicted in Fig. 8(a), when the HPM pulse is a sinusoidal signal with a frequency of 1 GHz, a pulse width of 10 ns, and a voltage amplitude of 1.5 V, the source current of the reinforced structure is more than ten times lower than that of the conventional structure. As shown in Fig.

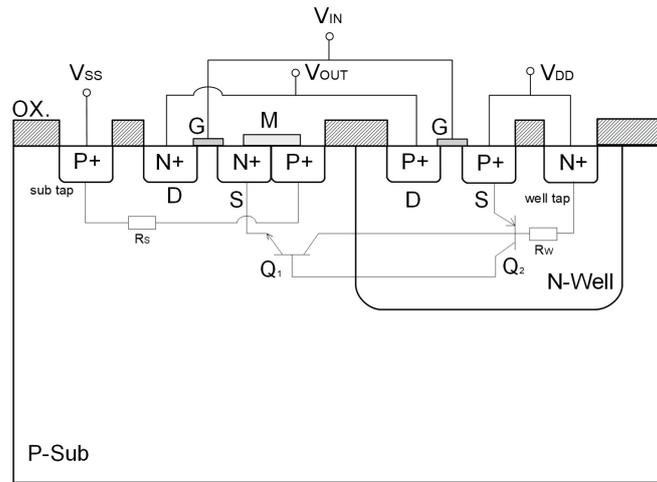


Fig. 7. Basic schematic of reinforced CMOS inverter.

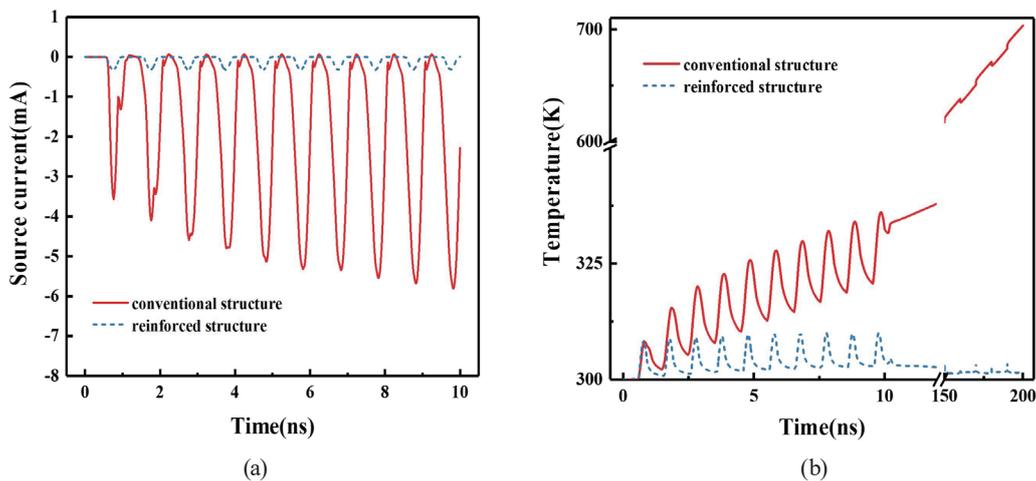


Fig. 8. (Color online) Variations of (a) source current and (b) peak temperature versus time in two cases.

8(b), the peak temperature changes within 200 ns were compared between the reinforced structure and the conventional structure. After the HPM pulse is removed, the temperature of the reinforced structure gradually drops to around 300 K, while the temperature of the conventional structure continues to increase. This shows that the reinforced structure can restrain the latch-up effect well.

The layout of the reinforced structure is shown in Fig. 9. Layout structure 100 includes P-substrate 101, on which N-well 102 is formed. Active region 103 of the N-channel MOSFET is formed in P-substrate 101. p-Type active region 104 is formed on the right side of the source region of the N-channel MOSFET. Regions 105 and 106 are the contact regions of the P-substrate and N-well, respectively. Active region 107 of the P-channel MOSFET is formed in N-well 102. The N-channel and P-channel MOSFETs share gate 108. Regions 109, 110, and 111 are the mask areas of p-type implantation, whereas 112 and 113 are the mask areas of n-type implantation.

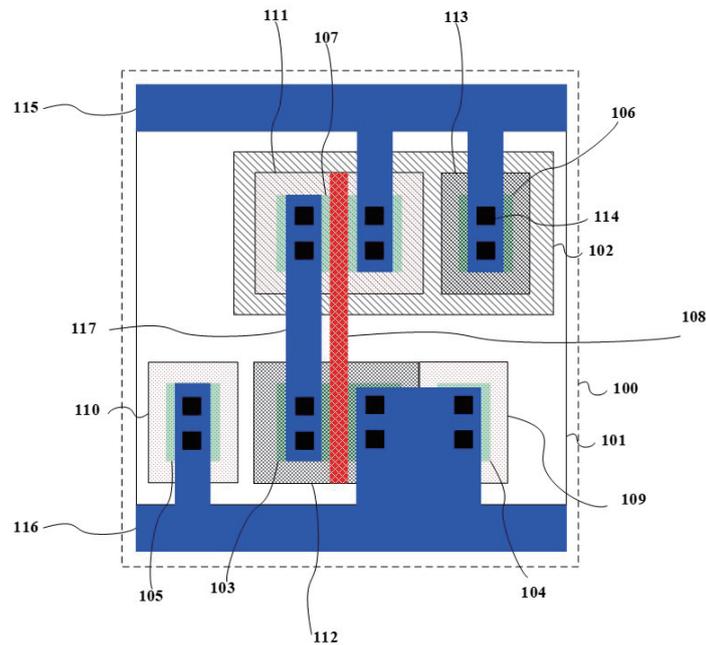


Fig. 9. (Color online) Schematic of simulation circuit.

Region 114 shows the contact holes that connect the semiconductor to the metal. Regions 115, 116, and 117 are the power line, ground line, and signal line, respectively.

4. Conclusions

In this study, the electrothermal coupling model of the 55 nm CMOS inverter was constructed. By studying the temperature and current characteristics, the failure mechanism of the CMOS inverter under the influence of the HPM pulse was elucidated. It was found that the latch-up effect is the main cause of the CMOS inverter damage. As a result of the examination of the failure process under different conditions, a reinforced structure that does not need additional process steps or conditions of the CMOS process is proposed. This reinforced structure can effectively reduce not only the influence of parasitic parameters, but also the number of electrons injected into the substrate when the HPM pulse is exerted. Research results showed that the source injection current of the reinforced structure under HPM interference is more than ten times lower than that of the conventional structure, effectively suppressing the latch-up effect. The reinforcement technology can provide anti-electromagnetic interference capabilities for sensors and other products based on the CMOS circuit.

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