

Influence of Environmental Conditions on Electrical Stability of Pentacene Thin-film Transistors with Cross-linked Poly(4-vinylphenol-co-methyl methacrylate) Gate Dielectric Layer

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Gate-bias stress causes changes in the electrical stability of thin-film transistors (TFTs), and this can degrade the device performance. This research highlights the effects of environmental conditions on the electrical stability of pentacene TFTs in which cross-linked poly(4-vinylphenol-co-methyl methacrylate) (PVP-co-PMMA) was utilized as a gate dielectric layer. Under negative gate-bias stress, the fabricated TFTs exposed to ambient air showed a positive threshold voltage shift, whereas the devices under vacuum exhibited a negative threshold voltage shift. Furthermore, consecutive on/off switching operation of pentacene TFTs under ambient air induced an increase in the on-state drain current. These results are explained through the interaction between water molecules and PVP-co-PMMA, which causes the accumulation of holes in the TFT channel region having higher conductance.

1. Introduction

Organic thin-film transistors (TFTs) have been extensively studied owing to their low-cost manufacturing process, processability at low temperatures, and mechanical flexibility, of which the latter allows them to be fabricated on plastic substrates. Dominant applications based on organic TFTs include driving elements of flexible displays, radio frequency identification tags, and several sensors.^(1–3) In particular, pentacene-based organic TFTs are promising owing to their ability to form well-ordered films on numerous substrates with high field-effect mobility.⁽⁴⁾ The structural and morphological properties of vacuum-deposited pentacene layers are governed by growth parameters such as the nature of the substrate, surface energy, roughness, temperature, and deposition rate.⁽⁵⁾ It is commonly known that the electronic performance of pentacene TFTs mainly depends on the grain size, crystallinity, and molecular orientation. Enormous progress has been made in enhancing their field-effect mobility and subthreshold characteristics.⁽⁶⁾ However, the stability of pentacene-based organic TFTs during operation under different environmental conditions is crucial for commercial electronics.

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Regarding the electrical stability issue, a continuous bias stress induces changes in the electrical characteristics of organic TFTs, particularly in the drain current and threshold voltage. Earlier studies have explained the difference in origin between the higher drain current observed in air than that observed in vacuum. Jung *et al.* reported that the increase in the drain current in air is due to the accumulation of extra charge carriers caused by the polarization of the insulator surface.⁽⁷⁾ Backlund *et al.* reported the ion-assisted modulation of the source-drain current of transistors.⁽⁸⁾ However, a decrease in the drain current in air was also reported and explained as having been caused by the capture of the charge carriers in the active channel by water molecules.⁽⁹⁾ In addition, a shift in the threshold voltages under gate-bias stress has been reported, and various mechanisms have been proposed to explain it: charge trapping in the dielectric or semiconductor, deep trap states in both the contact and active channel regions, and migration of the mobile ions.^(8–12) Taking into account the operation frequency of sensor circuits having a TFT amplifier and TFT switch, the electrical stability of TFTs is of prime importance for realizing high-performance sensors with fast signal processing and reliable sensing capabilities.

In this work, we studied the electrical stability of pentacene TFTs with cross-linked poly(4-vinylphenol-co-methyl methacrylate) (PVP-co-PMMA) as the gate dielectric in both ambient air and vacuum environments. The drain current and threshold voltage shift were examined as functions of the bias stress time and consecutive on/off switching operations in both the environments. The experimental results are explained through the interaction between the water molecules in ambient air and hydroxyl groups in PVP-co-PMMA.

2. Materials and Methods

For this study, bottom-gate and top-contact structured pentacene TFTs were fabricated on glass substrates. A schematic cross-sectional view of the TFTs used in this study is shown in Fig. 1(a). For the TFT fabrication, glass substrates ($2 \times 2 \text{ cm}^2$) were inserted in a rack and sequentially cleaned by ultrasonication in acetone, isopropanol, and deionized water for 15, 15, and 30 min, respectively. Nitrogen gas was blown onto the cleaned substrates; subsequently, the substrates were dried in an oven for 1 h at 180 °C. The gate electrodes were formed by vacuum evaporating 25-nm-thick Al at a rate of 0.1 nm/s. Here, PVP-co-PMMA was dissolved in propylene glycol methyl ether acetate (PGMEA), with poly(melamine-co-formaldehyde) (PMF) added to it as a cross-linking agent; the molecular structure of PVP-co-PMMA is shown in Fig. 1(b). The concentration ratios of the PVP-co-PMMA and PMF in the PGMEA solvent were both 15 wt.%. To fabricate a cross-linked PVP-co-PMMA gate dielectric layer, the PVP-co-PMMA solution was spin-coated at a speed of 2000 rpm and annealed at 210 °C for 1 h. Pentacene was used to form a 50-nm-thick active layer on the gate dielectric using thermal evaporation; the molecular structure of pentacene is shown in Fig. 1(c). Lastly, 50-nm-thick Au source and drain electrodes were formed on top of the active channel using thermal evaporation through the mask. The channel width and length of the fabricated TFTs were 800 and 100 μm , respectively.

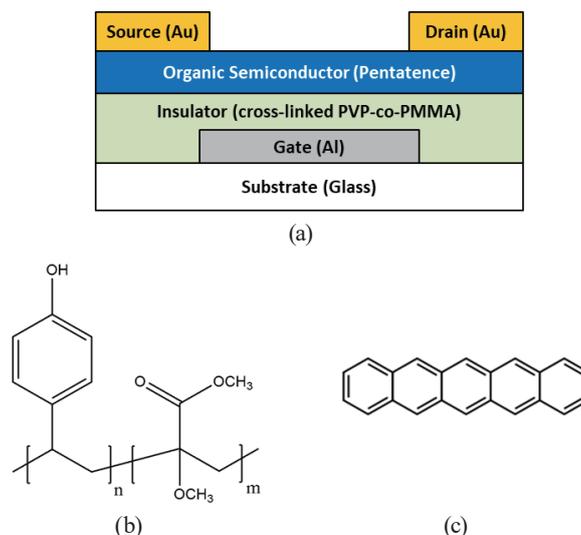


Fig. 1. (Color online) (a) Cross-sectional schematic of the fabricated pentacene TFT and chemical structures of (b) PVP-co-PMMA and (c) pentacene.

3. Results and Discussion

3.1 Structural characteristics of pentacene and cross-linked PVP-co-PMMA films

3.1.1 Morphological properties

Atomic force microscopy (AFM) is used to understand the structural morphology of the cross-linked PVP-co-PMMA dielectric layer. An AFM micrograph of the PVP-co-PMMA film is shown in Fig. 2(a). It is observed that the cross-linked PVP-co-PMMA exhibits a smooth surface morphology with a root mean square (RMS) roughness value of 0.33 nm. The obtained smooth surface might be due to the uniform distribution of the polymer on the gate electrode achieved by using the spin coater at the specified rpm. The smooth and well-distributed polymer film is essential as it can significantly influence the device performance and the growth of a pentacene film with a large grain size, which could eventually lead to higher mobility in TFTs.^(13–15) An AFM surface image of the pentacene film deposited on the cross-linked PVP-co-PMMA dielectric layer is shown in Fig. 2(b). As can be observed from the figure, the pentacene layer on the polymer film exhibits dendritic structures with larger grain sizes. Thus, it is observed that the pentacene film surface has a coarse morphology with an RMS roughness value of 15.59 nm. The uniformly formed dendritic structures with larger grain sizes are mainly due to the smooth surface of the polymer film. Importantly, the well-ordered pentacene molecules with larger grain sizes can reduce the trap distribution width.⁽¹⁵⁾

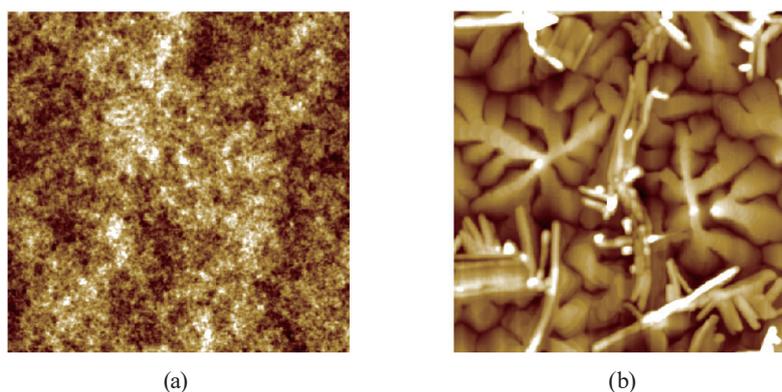


Fig. 2. (Color online) AFM images ($3 \times 3 \mu\text{m}^2$) of (a) cross-linked PVP-co-PMMA and (b) pentacene films.

3.1.2 Crystalline properties

The crystallinities of the cross-linked PVP-co-PMMA and pentacene films were examined using X-ray diffraction (XRD). The crystallinity of pentacene molecules deposited on a cross-linked PVP-co-PMMA film is known to be strongly influenced by the surface roughness of the gate dielectric layer.⁽¹⁶⁾ The XRD patterns of the polymer and pentacene films are shown in Fig. 3. From Fig. 3(a), it can be observed that there is no diffraction peak formed for the cross-linked PVP-co-PMMA, which might be due to the amorphous nature of the polymer even after the cross-linking process.⁽¹⁷⁾ Figure 3(b) shows the XRD pattern of the pentacene film thermally deposited on the cross-linked PVP-co-PMMA film. As seen, the pentacene film exhibits six distinctive sharp crystalline peaks. In detail, the pentacene film exhibits a series of well-defined (001'), (002'), (003'), and (004') peaks, which agree well with the typical (00l') pattern of the pentacene thin-film phase crystallites. The ($\bar{1}11$, 110) peaks generated from the lamellar grains and the (004) peak generated from the bulk phase crystallites were observed at $2\theta = 19.3^\circ$ and $2\theta = 24.1^\circ$, respectively.

3.2 Electrical characteristics of pentacene TFTs fabricated with cross-linked PVP-co-PMMA

3.2.1 Output characteristics of the pentacene TFTs

The output characteristics of the TFTs were measured in air and under vacuum by varying the drain voltage from 0 to -30 V in -1 V increments at different gate voltages. Figure 4 shows the obtained output characteristics of the pentacene TFT under both atmospheres. The maximum drain currents of the TFTs in air and under vacuum are approximately -0.10 and $-0.06 \mu\text{A}$, respectively. It is observed that the fabricated pentacene TFT exhibits higher drain current in ambient air than in vacuum. From these observations, we attribute this drain current enhancement in air to the ions originating from the interaction of water molecules that may have diffused through the grain boundaries of the pentacene layer, along with the hydroxyl ($-\text{OH}$) groups of the cross-linked PVP-co-PMMA dielectric layer. This reaction

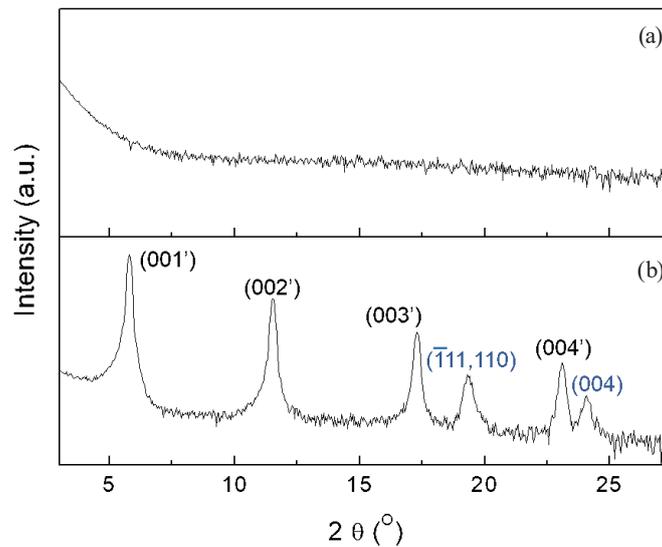


Fig. 3. (Color online) XRD patterns of (a) cross-linked PVP-co-PMMA and (b) pentacene films.

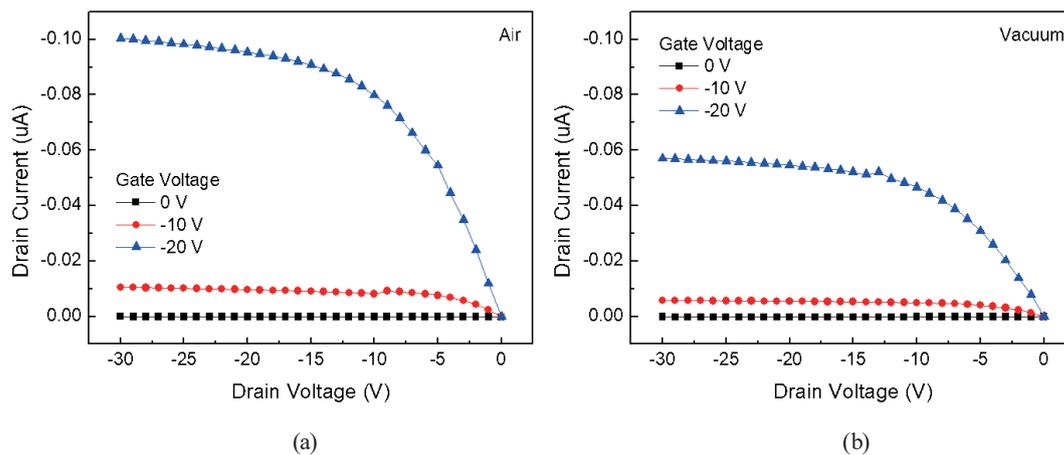


Fig. 4. (Color online) Output characteristics of the pentacene TFT (a) in ambient air and (b) under vacuum.

results in the formation of polymeric negative ions, i.e., $-O^-$ ions, at the cross-linked PVP-co-PMMA/pentacene interface. Previously, humidity has been shown to degrade the drain current in pentacene-based TFTs with PMMA dielectric material in ambient air owing to charge trapping at grain boundaries by the polar water molecules, thereby reducing the rate of charge transportation. However, in this study, the superimposition of the polymeric negative-ion-induced current onto the electronic current outweighs this effect, indicating that the trapping of charge carriers at the semiconductor/insulator interface plays a negligible role. Similarly, the experimental results from the literature also support the reasoning that the cause of the enhanced drain current in organic TFTs is the influence of water molecules, and more importantly, that the mechanism follows a reversible reaction without any assistance from external factors.⁽⁵⁾ Although the hydroxyl groups are substituted by the PMF cross-linking agents, it is not possible to completely remove the hydroxyl groups. These unsubstituted

hydroxyl groups might change the drain current of pentacene TFTs. It should be noted again that the maximum drain current under vacuum is lower owing to the absence of air molecules. Overall, it can be concluded that the water molecules in ambient air strongly influence the electrical characteristics in pentacene TFTs.

3.2.2 Gate-bias stress on pentacene TFTs

Organic TFTs are known to have stability issues caused by the gate-bias stress, which can eventually degrade the device performance by an undesirable (spontaneous) shift in the threshold voltage. To generate a negative gate-bias stress, we applied a constant gate voltage of -30 V for an extended time period (1000 s) while the source was grounded and the drain potential was set at 0 V. After applying a negative gate-bias stress for each stress time, we measured the transfer characteristics of the pentacene TFT by sweeping the gate voltage from 15 to -30 V in increments of 0.5 V with a fixed drain voltage of -30 V. In air, as shown in Fig. 5(a), the drain currents in both the off and on states continuously increase during the application of negative gate-bias stress. In contrast, there is no discernible change in the slope of the transfer curves in Fig. 5(b), i.e., the plots of $|\text{drain current}|^{1/2}$ versus gate voltage; this indicates that the field-effect mobility of the TFT was not affected by the gate-bias stress.^(7,8) Figure 5(c) summarizes the extracted threshold voltages based on the bias-stress time; it can

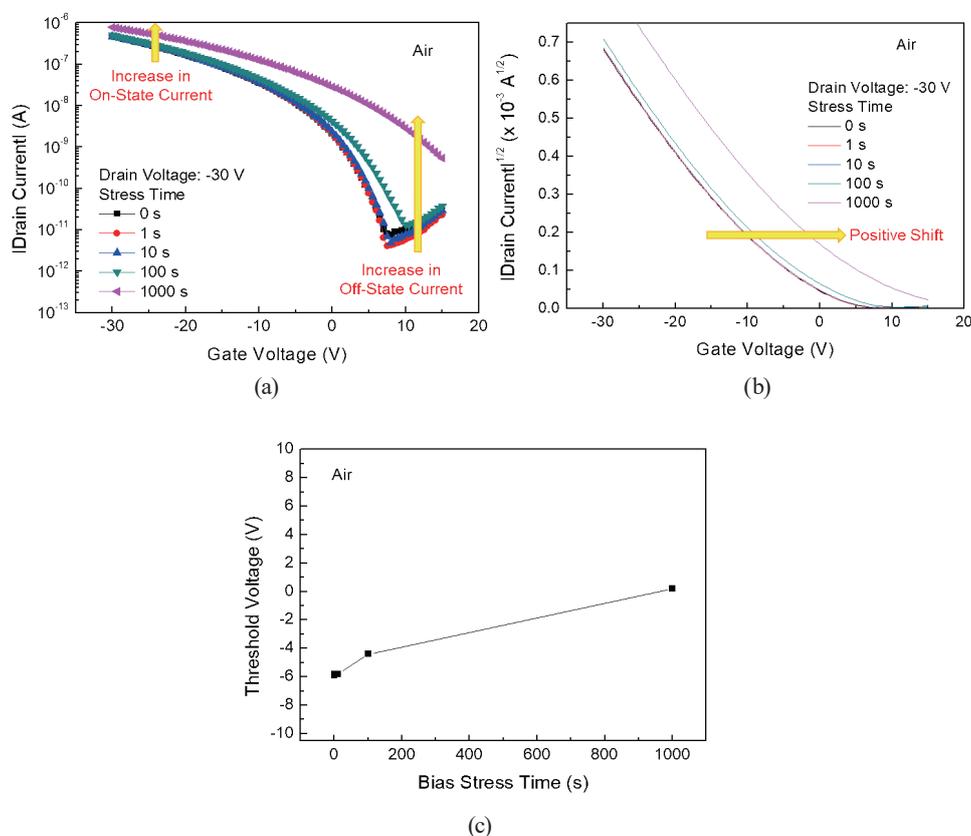


Fig. 5. (Color online) Transfer curves of (a) $|\text{drain current}|$ versus gate voltage and (b) $|\text{drain current}|^{1/2}$ versus gate voltage. (c) Variation in the threshold voltage with time as a result of the negative gate-bias stress.

be seen that the threshold voltage shifts towards the positive direction with an increase in the gate-bias stress time. The observed positive shift in threshold voltage may indicate that the charge-trapping mechanism in the semiconductor or the semiconductor/dielectric interface layer has a negligible effect. This shift occurred owing to the absorption of water molecules by the hydroxyl groups in the cross-linked PVP-co-PMMA (gate dielectric) material.^(18,19) It should also be noted that the increase in the saturation drain current cannot be attributed to the charge trapping behavior. Herein, a possible cause of the threshold voltage shift and higher drain current might be the creation of polymeric negative ions (O^- ions) in the cross-linked PVP-co-PMMA dielectric layer, which cause excess holes and thus increase the conductivity of a channel. Polymeric negative ions at the gate dielectric surface generate an electric field that is superimposed on the one generated by the gate bias, and reveals itself electrically via a positive shift of the threshold voltage. As shown in Fig. 5(c), the threshold voltage shifts by approximately 2 V during the first 100 s, which is rapid compared with the approximately 4 V shift in the next 900 s. This behavior can be attributed to the chemical reaction rate of the water and dielectric, which decreases with time as it approaches the equilibrium point. This means that in the first 100 s, the rate of ion generation leads to the addition of charges on the semiconductor. Nevertheless, this reaction seems to be reversible because the ionic effect vanishes when devices are characterized under vacuum. As shown in Fig. 6, the TFT under

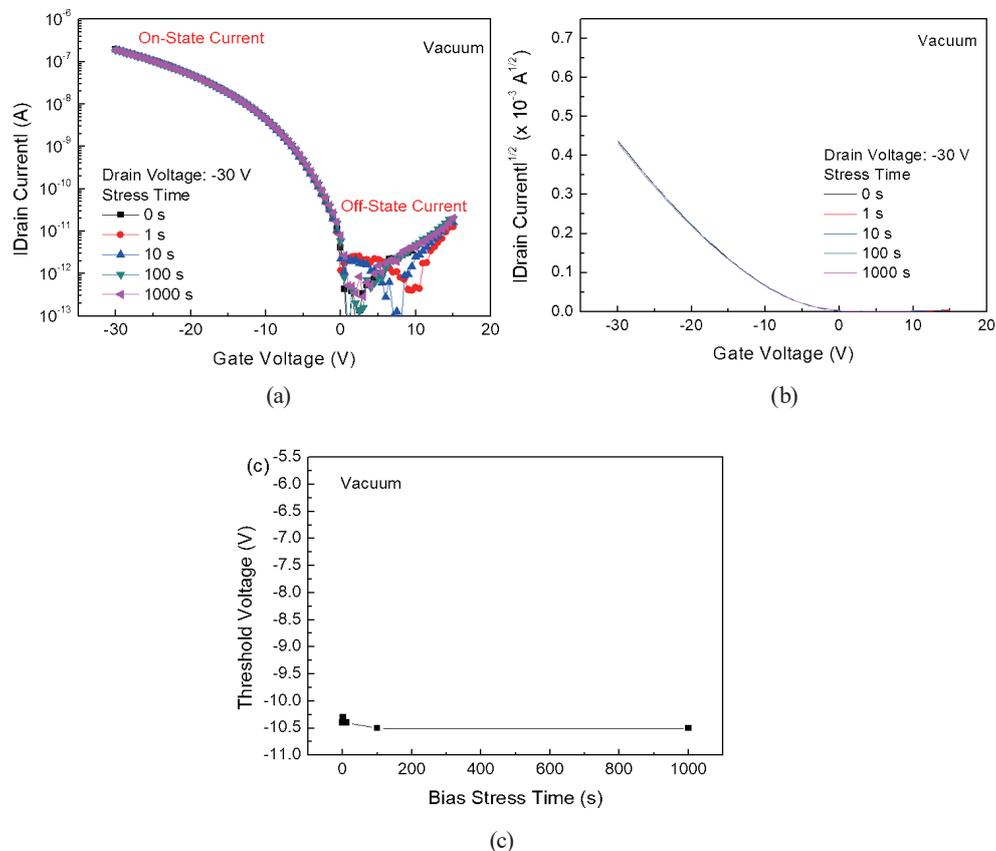


Fig. 6. (Color online) Transfer curves of (a) |drain current| versus gate voltage and (b) |drain current|^{1/2} versus gate voltage. (c) Variation in the threshold voltage with time as a result of the negative gate-bias stress.

vacuum exhibits a negligible threshold voltage shift for the same negative bias stress condition, suggesting that the bias stress without media has no impact on the electrical stability of the TFTs.⁽¹⁸⁾ Therefore, it is clear that the hydroxyl groups and absorbed water molecules at the interface of the semiconductor and dielectric layer are the main causes of the threshold voltage shift in the pentacene TFTs. Therefore, the passivation or encapsulation of the TFTs is expected to pave the way for minimizing the air-induced degradation in the TFT performance.

3.2.3 Consecutive on/off switching operation of pentacene TFTs

Previous studies have reported only TFT performance changes in terms of environmental stability. However, the application of TFTs to sensor circuits requires the study of continuous switching operation. To reflect this requirement, the dynamic characteristics of the fabricated pentacene TFTs are examined through the consecutive on/off switching operation in this study. As shown in Fig. 7(a), pulses with a gate voltage of 0 V and drain voltage of 0 V were applied to switch the TFT off, and pulses with a gate voltage of -30 V and drain voltage of -30 V were applied to switch the TFT on. Figure 7(b) shows the dynamic response of the pentacene TFT in ambient air. As expected from the above results, the on-state drain current increased in ambient air during the consecutive on/off switching conditions. This increase is believed to be caused

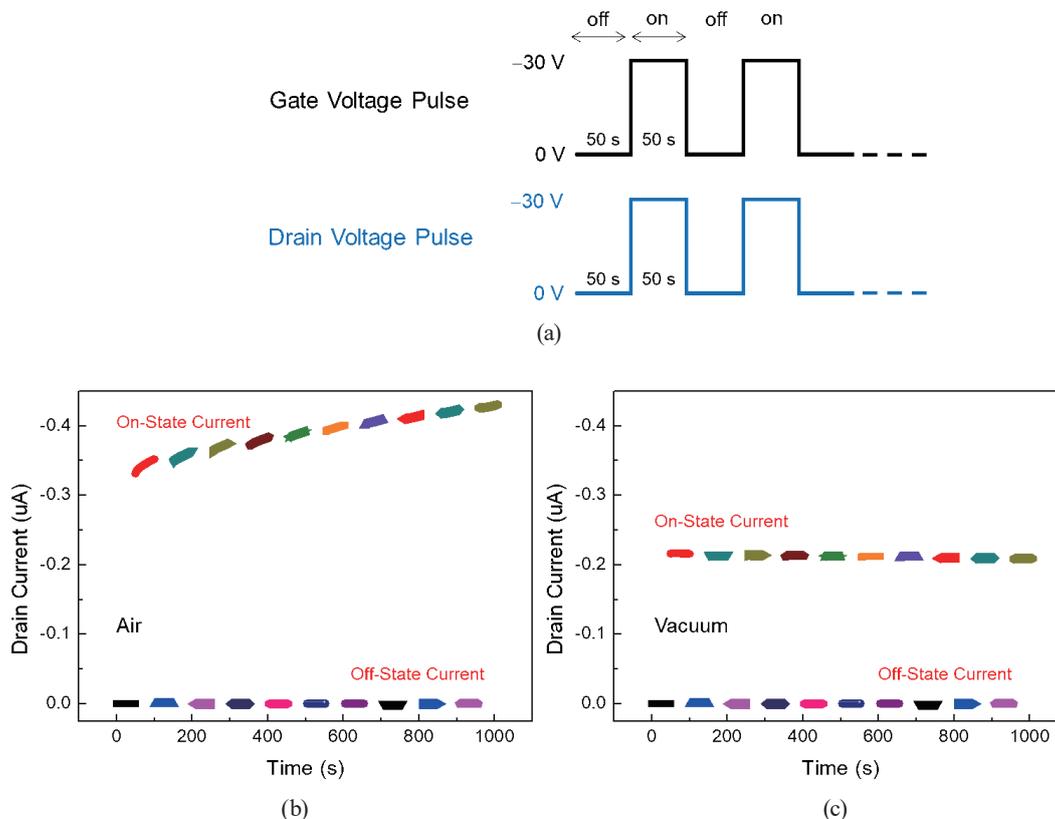


Fig. 7. (Color online) (a) Driving schemes of the gate voltage and drain voltage. Variation of drain current of pentacene TFT (b) in air and (c) under vacuum.

by the water molecules that generate electron acceptors under negative gate bias.⁽²⁰⁾ During the consecutive on/off switching operation of the pentacene TFTs, the concentration of polymeric negative ions increases as more water molecules are absorbed to interact with the cross-linked PVP-co-PMMA gate dielectric layer. However, there is no significant change in the on-state drain current under vacuum, as shown in Fig. 7(b). According to the results, the off-state drain currents in air and under vacuum remained comparable during the off period, indicating that the TFT was fully switched off under a gate voltage of 0 V. Thus, these results demonstrate that the water molecules present in air play an important role in the significant changes in the drain current.

4. Conclusions

The bias stress phenomena in top-contact pentacene TFTs with a cross-linked PVP-co-PMMA gate dielectric layer were investigated in both air and vacuum. The drain current in the initial state as well as in the bias state is higher in air owing to polymer surface polarization by the air molecules, which generate extra charge carriers, thereby increasing the conductivity of the active channel. We also reported a positive threshold voltage shift in ambient air, which is ascribed to the absorption of water molecules by the hydroxyl groups present in the gate dielectric material. Our experiment shows that the environment is crucial for the stable operation of organic TFTs because it affects their electrical properties. It was also confirmed that the environmental conditions have a strong influence on the electrical stability of TFTs. We expect that further research on the absorption and desorption behaviors of the water molecules at the interface between the polymeric gate dielectric and organic semiconductor will serve to optimize the driving scheme of organic TFT-based circuits.

Acknowledgments

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