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Modulation of Gate Work Function of Devices for Protection Against Electrostatic Discharge

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Electrostatic discharge (ESD) events are causing an increasing amount of damage in advanced integrated circuits (ICs). Among the onchip ESD protection devices, the silicon controlled rectifier (SCR) is the most robust. We have proposed a new SCR with an embedded n-type metal-oxide-semiconductor field-effect transistor (nMOSFET). By properly adjusting the gate work function of the nMOSFET, the SCR obtains a low trigger voltage of 1.5 V and a low leakage current of 7.6×10^{-10} A. The overshoot voltage under a fast ESD event is also reduced owing to the strong conduction of the nMOSFET. By numerical simulation, we evaluate the impact of the temperature, noise, and stress waveform on the ESD performance. The results are discussed and detailed physical insights are given.

1. Introduction

With the scaling down of the feature size of complementary metal-oxide-semiconductor (CMOS) technology, the thinner gate oxide and shallower junction are introducing new reliability issues for integrated circuit (IC) design. Therefore, preventing electrostatic discharge (ESD) has been acknowledged as one of the most urgent tasks in ensuring the reliability of CMOS ICs.[1–4] As part of the whole-chip ESD protection, the power clamp circuit is indispensable to prevent thermal breakdown in the internal circuit of ICs.[5–11] It provides a low-impedance path for each IC to discharge ESD energy from the power supply line (VDD) to the ground line (GND). A silicon controlled rectifier (SCR) can be used to construct a power clamp circuit; it has high robustness among the several widely used ESD protection devices since its parasitic cross-coupled bipolar junction transistors (BJTs) operate in positive feedback mode.[12,13] However, a conventional SCR cannot be directly used for low-voltage CMOS technology ICs, because its trigger voltage is very high and cannot protect the gate oxide effectively. Hence, ESD detection circuits should be added to help rapidly trigger SCR devices.

A typical RC-triggered power clamp circuit distinguishes ESD and normal power-up events by their different slew rates.[5,6] The RC time constant is usually set to 1 μs to meet the

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requirement for the human body model (HBM) discharge duration. This results in the risk of false triggering when fast power ramps exist. Another widely used detection method is based on a diode string, which is classified as a voltage detection mechanism. When the voltage on the VDD exceeds the threshold voltage (Vth) of the diode string, the clamp circuit or device is turned on to discharge the current.[14–19] However, the diode string may introduce a high leakage current, especially at high temperatures. Both the above two solutions occupy extra layout area. The well-known low-voltage-triggered SCR (LVTSCR) is area-efficient, but the trigger voltage should be further reduced to make it suitable for advanced low-voltage technologies.[12,13]

In this study, an SCR device with a new voltage detection method is proposed. Since an n-type metal-oxide-semiconductor field-effect transistor (nMOSFET) with a modulated gate work function is embedded into the SCR device, a low trigger voltage and a low leakage current can be obtained. The operating principle of the new device is investigated by technology computer-aided design (TCAD) simulation. The impact of the temperature, noise, and stress waveform on the new device is also discussed.

2. Device and TCAD Methodology

2.1 Device design

A cross-sectional view of a traditional LVTSCR is shown in Fig. 1(a). It can be seen that an nMOSFET (nMOS1) with a normal gate work function is embedded into an SCR device. The gate of nMOS1 is grounded, namely, nMOS1 is constantly off. Thus, the trigger mechanism remains avalanche breakdown. When the anode voltage is sufficiently high, the drain/substrate junction breaks down and the trigger voltage is reduced to around 7 V. A new SCR, which includes parasitic npn and pnp BJTs, is proposed, whose cross-sectional view is shown in Fig. 1(b). The differences between the two SCRs are the gate connection and gate work function; the nMOSFET in the proposed SCR has a higher Vth and the gate is connected to the anode. The gate work function can be selected in advanced CMOS technologies; thus, the proposed device is compatible with these technologies.[20]

The equivalent circuits of the two SCRs are shown in Figs. 1(c) and 1(d). Vth of nMOS2 in the proposed SCR is higher than that of nMOS1 in terms of the operating voltage (1 V in this work), ensuring that nMOS2 is in the OFF state under normal operating conditions. When an ESD event occurs, the voltage on the VDD exceeds the normal operating voltage, and nMOS2 starts to conduct and turns on the SCR. The p+/N-well junction (emitter-base junction of the parasitic pnp BJT) in the SCR's anode and nMOS2 form a trigger path, and the SCR can be quickly turned on.

The parameters of the device studied in this work are as follows: thickness of gate oxide: T_{ox} = 4 nm, depth of source and drain regions: X_j = 30 nm, lengths of anode p+ and cathode n+ regions: $L_{AP} = L_{CN}$ = 300 nm, lengths of gate and nMOS2's drain regions: $L_G = L_D$ = 200 nm. The doping concentrations of the n+ region, p+ region, n-well, and p-substrate are 1×10^{20}, 1×10^{20}, 1×10^{17}, and 1×10^{17} cm^{-3}, respectively. The gate work functions of the normal- and

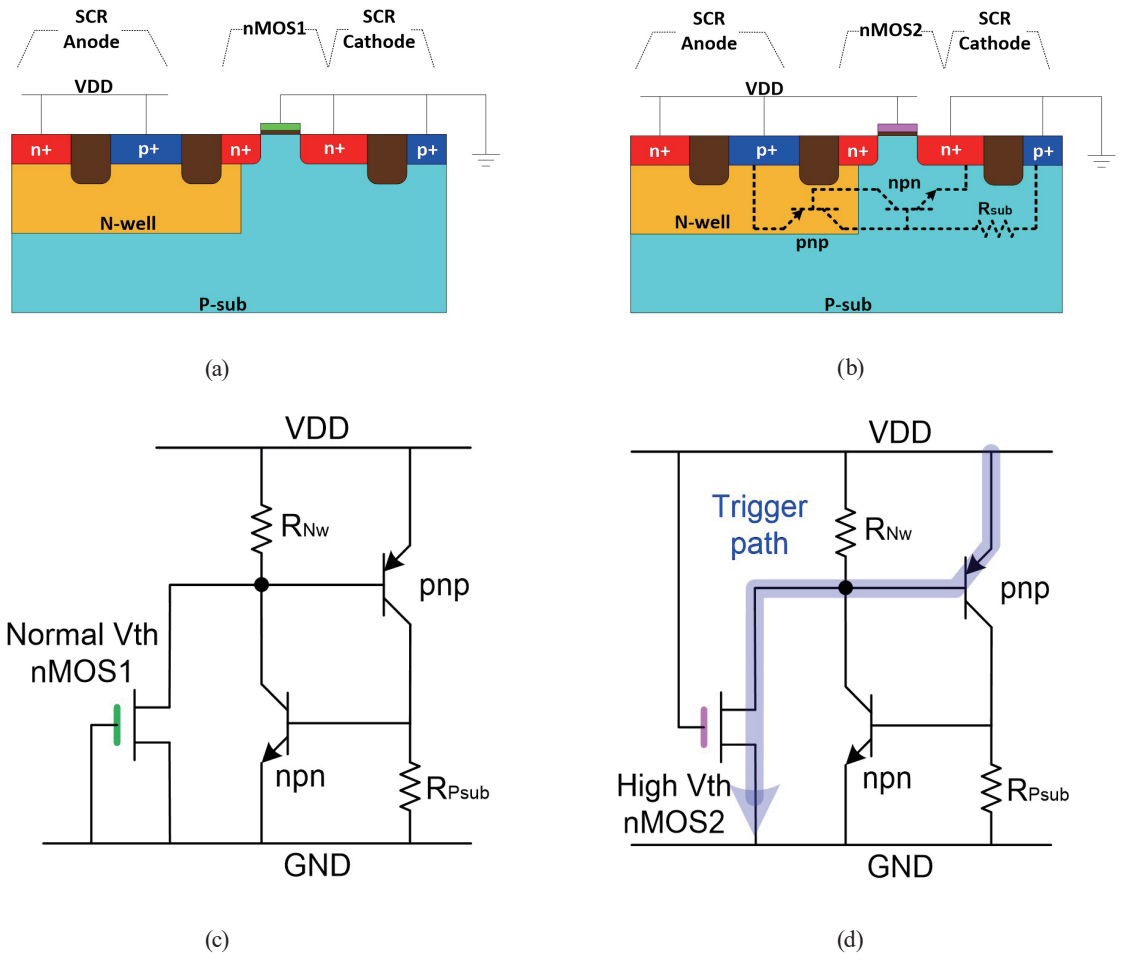


Fig. 1. (Color online) Cross-sectional views of (a) traditional LVTSCR and (b) proposed SCR. Equivalent circuits of (c) traditional LVTSCR, and (d) proposed SCR.

high-Vth nMOSFETs are 4.3 and 5.3 eV, respectively. The material of the gate oxide and trenches is SiO_2. The width of the device is 50 μm. The thermal boundary conditions are very important in ESD simulation, and unsuitable conditions may produce incorrect results. Since the thermal diffusion length of the silicon devices for 100 ns ESD simulation is approximately 3 μm, the substrate thickness T_{Sub} is chosen to be 3 μm. All the terminals are used as a heat sink. The surrounding temperature of the device is set as 300 K.

2.2 TCAD methodology

The simulations in this study are carried out in a Sentaurus TCAD simulator. High-field saturation and Philips Unified models are used to calibrate the carrier mobility. The Van Overstraeten model is used to calculate the effect of impact ionization. A thermodynamic model is used to calculate the lattice temperature. The Shockley–Read–Hall recombination model and a bandgap narrowing model are also used.

The transmission line pulsing (TLP) test method is used to simulate the quasistatic *I*–*V* characteristics of the devices. The rise time and pulse width of the current waveform are set at 10 and 100 ns, whereas for the very fast TLP (vfTLP), the two values are 0.2 and 5 ns, respectively.

The transfer curve of the nMOS with a gate work function of 5.3 eV used in the simulation is shown in Fig. 2. V_{DS} is fixed at 1 V, and the currents with V_{GS} of 1 and 2 V are 2.1×10^{-10} and 5.8×10^{-4} A/μm, respectively.

3. Results and Discussion

3.1 Normal power-up event

Since nMOS2 is designed to have a high Vth, it does not conduct under the normal operating voltage bias. Thus, the SCR cannot be turned on, and the leakage current is mainly composed of the subthreshold conduction of nMOS2. A voltage waveform with 1 μs rise time and 1 V amplitude is applied to the VDD to simulate the normal power-up event. The simulation results in Fig. 3(a) show that the highest current during the power-up event is 59 nA, which quickly

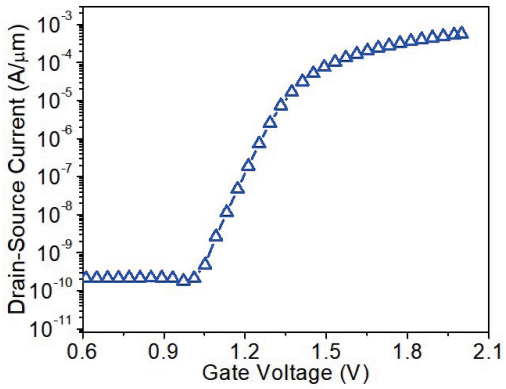
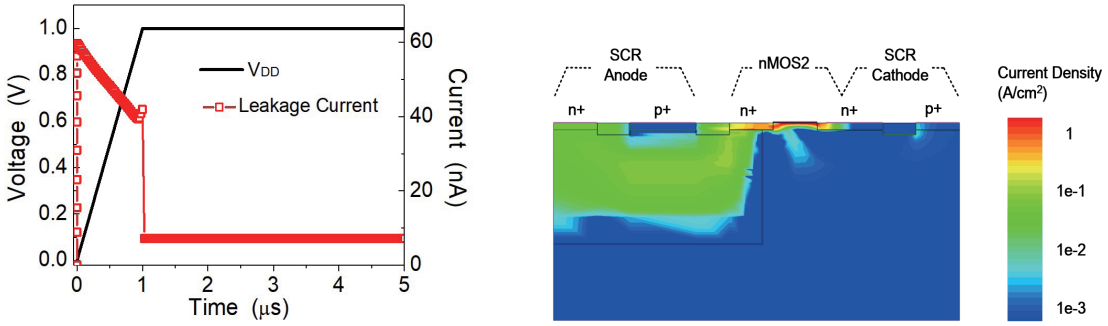


Fig. 2. (Color online) Transfer curve of the nMOS used in this work.



(a) (b)

Fig. 3. (Color online) (a) Leakage current under a power-up event and (b) contour plot of the current density when the VDD is stable.

drops to 7.6 nA, then remains at this value when the VDD becomes stable. Figure 3(b) shows that the leakage current flows from the anode's n+ region to nMOS2, and finally to the ground.

3.2 ESD event

The ESD current is injected into protection devices in a very short time (less than 10 ns), resulting in a high voltage. In the proposed device, the high voltage on the VDD quickly turns on nMOS2 since its gate is tied to the VDD. Therefore, nMOS2 generates a trigger current, the emitter-base junction of the pnp BJT is forward biased, and the positive feedback of the SCR can be established.

TLP simulation is widely used to evaluate the performance of ESD devices. In this work, current pulses with 10 ns rise time and 100 ns pulse width are applied to the anode of the SCR while the cathode is kept grounded. Figure 4 shows the response under a 1 A TLP stress. It can be seen that the first peak voltage is only 1.6 V at 1 ns, indicating that the positive feedback of the SCR is quickly established. The voltage on the VDD is clamped below 1.8 V. The maximal lattice temperature reaches 700 K at 100 ns.

Figures 5(a) and 5(b) show contour plots of the current density at different times during the stress. It can be seen that the trigger path is from the p+/N-well junction to nMOS2, which verifies the above analysis. At 90 ns, the current path is mainly distributed in the bulk of the device rather than at the surface of the silicon, indicating that SCR conduction is dominant.

On the basis of the results of a series of TLP simulations, the TLP curve of the proposed device is drawn in Fig. 6. The quasistatic *I*–*V* characteristic is obtained by averaging the transient data in the interval of 60 to 90 ns. The simulation is terminated when the maximal lattice temperature reaches 1500 K. It can be seen that the proposed circuit has a very low trigger voltage of 1.53 V and a high failure current of 3.5 A.

3.3 Noise characteristics

The power clamp circuit can be falsely triggered under a noise pulse, which may lead to a large current and cause damage. In this work, since an nMOSFET is embedded into the SCR, the noise immunity should be considered. To simulate the device characteristic under a serious noise environment, ±10% VDD (0.1 V) variations in 1 ns are applied to the VDD. Figure 7 shows that

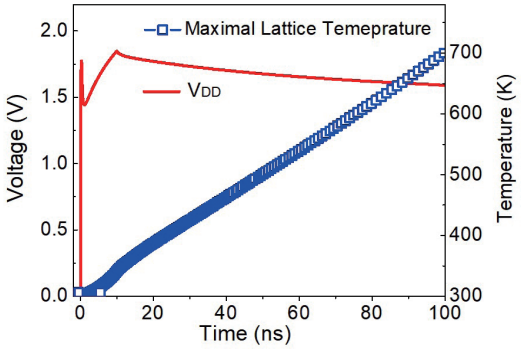
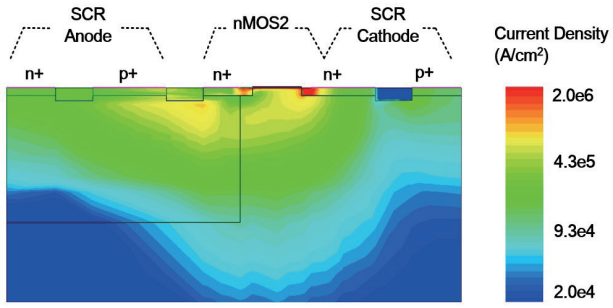
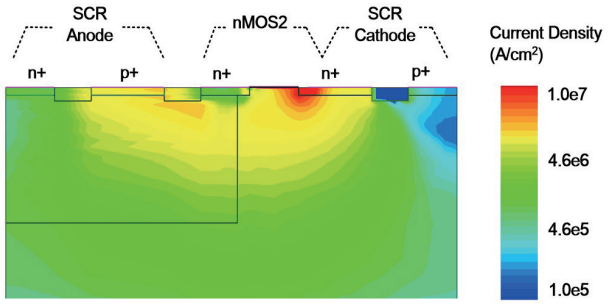


Fig. 4. (Color online) Waveforms of VDD and maximal lattice temperature during 1 A TLP simulation.



(a)



(b)

Fig. 5. (Color online) Contour plots of current density at (a) 0.5 ns and (b) 90 ns under a 1 A TLP stress.

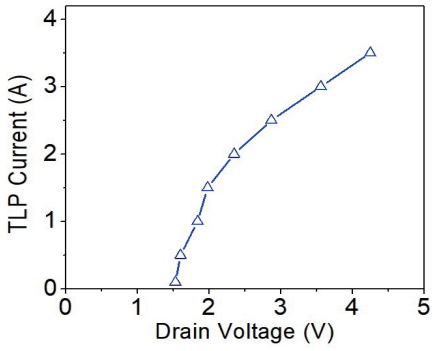


Fig. 6. (Color online) TLP *I*–*V* curve of the proposed device.

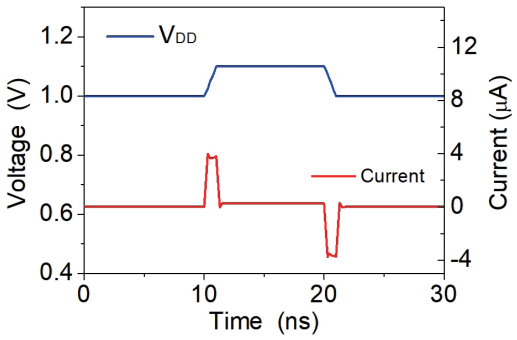


Fig. 7. (Color online) Noise characteristic of the proposed device.

with such a fast transient, the peak current is only around ±4 μA and returns to the normal value quickly. Thus, the proposed device has high noise immunity.

3.4 Impact of temperature

When an IC is under normal operation, the ambient temperature may increase due to the Joule heat generated in semiconductor devices. The main impact of a high temperature on the

proposed device is an increase in the leakage current and trigger voltage. Figure 8 shows that the leakage current increases from 7.6 to 1.93 μA when the temperature is increased from 25 to 125 °C.

3.5 Impact of current rise time

Fast ESD events, such as charged device model (CDM) events, are causing increasing damage to ICs. The most significant behavior of ESD devices under fast ESD events is voltage overshoot at the initial time. vfTLP currents with a rise time and pulse width of 0.2 and 5 ns, respectively, are applied to several devices for analysis. In addition to an LVTSCR and the proposed SCR shown in Fig. 1, a voltage-triggered SCR is also included for comparison as shown in Fig. 9. This voltage-triggered SCR can be regarded as an optimized LVTSCR, whose gate is modulated by a voltage detector consisting of a diode string and a resistor. When the voltage on the VDD is

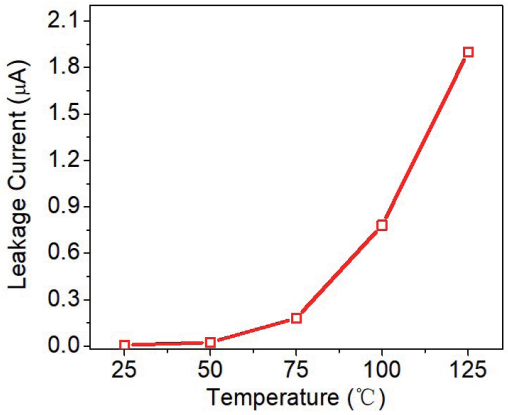


Fig. 8. (Color online) Leakage current at different temperatures.

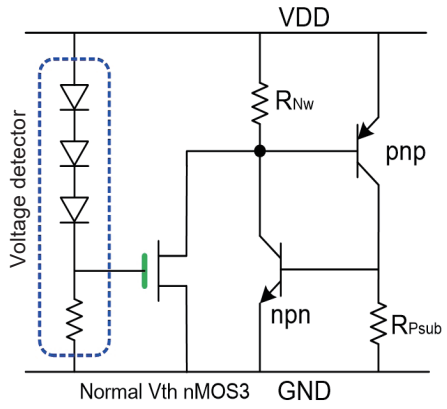


Fig. 9. (Color online) Schematic of a voltage-triggered SCR.

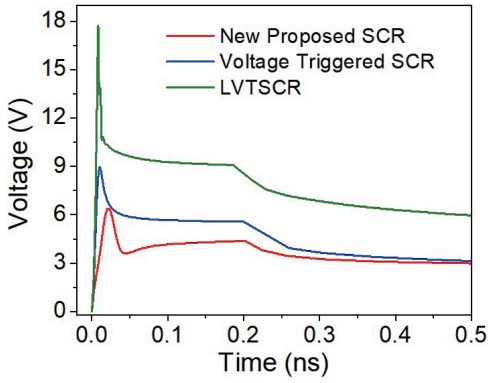


Fig. 10. (Color online) Waveforms of VDD of several devices in vfTLP simulations with 2 A amplitude.

sufficiently high, the diode string conducts, the gate of nMOS3 is elevated, nMOS3 starts to conduct, and finally the SCR is turned on. Owing to the gate voltage modulation, the voltage-triggered SCR establishes positive feedback more quickly than the LVTSCR.

The simulation waveforms of the three devices under a 2 A vfTLP stress are shown in Fig. 10. The results reveal that the proposed circuit has the lowest overshoot voltage. This can be attributed to the large gate-source voltage of nMOS2 and its strong conduction. The overshoot voltage of the voltage-triggered SCR is also less than that of the LVTSCR; however, a voltage detector is required, which usually has a layout area larger than the SCR itself and introduces more leakage current.

4. Conclusions

In this work, a new CMOS-technology-compatible SCR device for ESD protection is proposed. An nMOSFET with a gate tied to the anode is embedded into the SCR, and the high gate work function ensures that the leakage current is ultralow even with the gate tied to the anode. Owing to the high trigger current provided by the nMOSFET, the proposed device has a low trigger voltage compared with its traditional counterpart. The result of TCAD simulations shows that the proposed device has a low trigger voltage, low leakage current, and high robustness.

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