Electrostatic Discharge Reliability Sensing of Ultrahigh-voltage N-channel Laterally Diffused MOSFETs Modulated by Different Operating Voltages

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In this paper, electrostatic discharge (ESD) reliability sensing components for use in ultrahigh- to low-voltage environments were fabricated via a Taiwan Semiconductor Manufacturing Company (TSMC) 0.5 µm ultrahigh voltage (UHV) bipolar-CMOS-DMOS (BCD) process. To understand the trend of the capability of different voltage components under ESD stress, we designed ESD sensing components that can be used at different voltages. These ESD sensing components will be implemented using a circular layout. By changing the drift region and Poly2 parameters with a fixed gate terminal, we proposed a new design with eight sets of parameters. As the length of the drain-side drift region (L_D) increases, the parasitic resistance of the drift region also increases, which will improve the ability of the device to withstand ESD currents. Eventually, to further analyze the ESD capability of the component, a transmission-line pulse (TLP) test system was used for the DUT. When L_D is 28 µm, the device is optimal. The I_{t2} of the device can reach 4.43 A. The FOM is also used to determine the ESD capability of the component, which can reach a maximum of 3.15×10^2 (A·V/µm²).

1. Introduction

With the development of semiconductor technology and the advancement of component processes, the area of commercial ICs has continually decreased. However, as the component area decreases, it is likely to cause more and more electrostatic discharge (ESD) damage events and partial circuit failures. In addition, ESD events can often easily cause internal damage to IC devices.[1–5] ESD failures of components are usually more severe at higher operating voltages. However, because the ESD energy is not very high, it is often difficult to detect ESD damage by optical microscopy (OM) especially for low operating voltages.[6–9] Therefore, high-voltage or ultrahigh-voltage (UHV) ESD protection designs must be applied in many power management circuits such as AC/DC converter circuits, automotive electronics, and liquid crystal displays

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(LCDs). To prevent ESD events from increasing the damage to components, we use TSMC 0.5 μm UHV process components for self-protection component designs in this study.[9–16] These UHV devices will be presented in a circular layout, and the final optimal design is expected to have high/ultrahigh-voltage components with different breakdown voltages and an excellent ESD capability in ESD sensing applications. It is hoped that the final designed components can be used as protection components under different operating voltages, and the ESD capability of these components is analyzed through TLP measurements.[17–25]

2. Device Structures

2.1 UHV n-channel laterally diffused MOSFET (nLDMOS) reference device

Figures 1(a) and 1(b) show the structure of the reference device for our design. To protect the IC I/O circuit, a gate-to-ground NMOS (GGNMOS) design was adopted for test purposes. Owing to the GGNMOS architecture, this MOSFET will not trigger conduction under normal conditions. However, this component is instead conducted by a parasitic bipolar junction transistor (BJT) path as in an EOS situation. Then, an UHV nLDMOS components is designed in a circular layout. The Poly2 layer is used to increase the breakdown voltage (and operating voltage) of the components, and it is designed to be spiral. The overall length of the Poly2 layer is easily increased by the spiral layout. Then, the drift region creates a large field-plate effect, which leads to an increase in breakdown voltage, which allows these devices to operate in UHV environments. Because the Poly2 layer is related to the floating condition, it reduces the on-state field. The buried N-well (BNW) layer is highly doped on top of P-sub, and its purpose is to form a reverse diode with P-sub to prevent the excessive leakage current from flowing to the P-sub region. The deep P-well (DPW) layer is also designed with a high-voltage N-well (HVNW) inside the component to form a RESURF, which increases the breakdown voltage of the component. The length of the drift region (L_D) is defined as the distance between the HVNW and the drain terminal N+, and is also the main subject of this work.
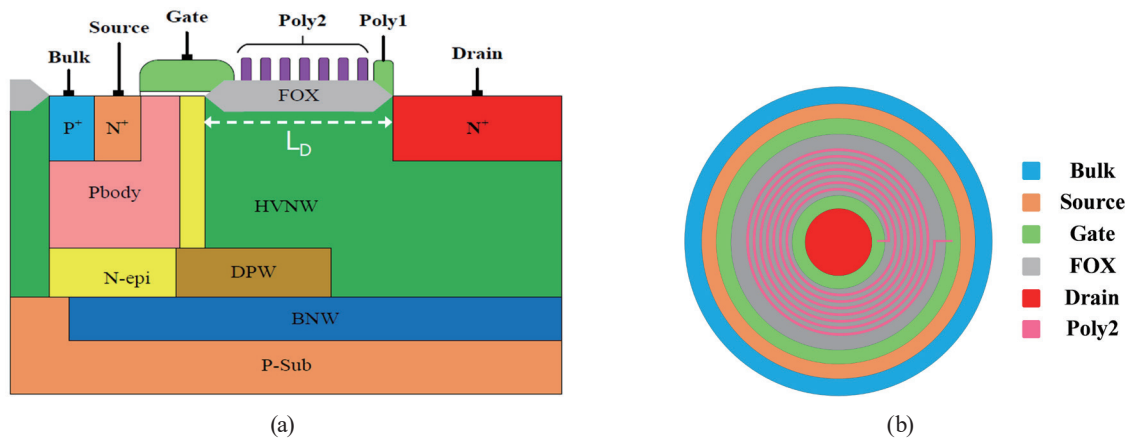

Fig. 1.   (Color online) (a) Cross section and (b) layout view of the UHV nLDMOS reference component.

2.2   Design devices for different operating voltages

To use the components in different operating voltage ranges, a reference device of components is used to adjust the component parameters. The component breakdown voltages are designed to be in the ranges of 100 to 200 V, 200 to 300 V, and above 300 V. As shown in Fig. 2(a), the breakdown voltage is adjusted by changing L_D and the number of turns of Poly2 (N_P). As L_D determines the size of the HVNW, the parasitic resistance (R_{HVNW}) on the HVNW will also be proportional to the HVNW zone in Fig. 2(b). As the length of the HVNW increases, the larger parasitic resistance due to the longer distance across the component causes the current density to decrease, and hence the ESD current flow is improved. To maintain the breakdown voltage in the operating voltage range, L_D is strongly related to the breakdown voltage. The drift region parameters are then designed according to the default voltage. As L_D decreases, this Poly2 reduces the number of turns in the drift region. The device modulation parameters are shown in Table 1. However, when the parameter of the drift region is less than 15 μm (S15_R), the Poly1 and metal layer parameters are considered to be the same. This results in the new device not having a Poly2 layer layout, which causes the loss of the field plate effect above the field oxide (FOX). This will cause the breakdown voltage to drop quickly and alter the linear relationship of the falling breakdown voltage.
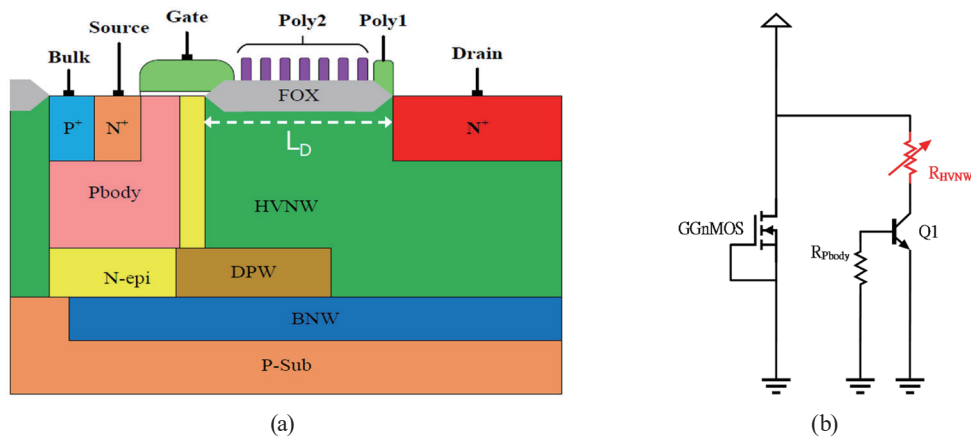

| (a) | (b) |

Fig. 2.   (Color online) (a) Cross-sectional view of UHV nLDMOS components and (b) equivalent circuit.

Table 1
Layer parameters of UHV nLDMOS components.

Cell name	N_p (turn)	L_D (μm)
S13_R	0	13
S14_R	0	14
S15_R	0	15
S18_R	1	18
S21_R	3	21
S24_R	5	24
S27_R	6	27
S28_R	7	28

Thus far, it has been found that if L_D is large, the I_{t2} capability of the device is effective. However, the component area increases and the chip cost is also higher. Therefore, the design factor of merit (FOM) can be used to analyze component capabilities and determine which component is better. The FOM can be determined as

$$FOM = V_h \text{ (V)} \times I_{t2} \text{ (A)} / \text{Cell Area (μm}^2), \tag{1}$$

where V_h is the holding voltage. This value is related to the ability to withstand the latch-up immunity. I_{t2} is the maximum secondary breakdown current that a component can withstand. By multiplying these two values, the reliability of the component can be more accurately determined by the ESD/latch-up capability of the design.

3.   Test Machines

First, it is necessary to know whether the operating voltage of the component is within the voltage range. We used the breakdown voltage to determine it. Here, a Keithley-2410 tester was used to measure the breakdown voltage (i.e., operating voltage) of devices as shown in Fig. 3(a). The DC breakdown voltage is measured by limiting the component leakage current. The breakdown voltage point is defined as the voltage when the leakage current of a device reaches 1 μA.

Next, a TLP system was used to analyze the ESD capability of the devices as shown in Fig. 3(b). ESD events quickly occur and the damage to the component is very significant. In other words, the TLP system is used to simulate the real human body model (HBM). The TLP system uses a fast square wave to zap the component. The rising and falling time of the square wave is approximately 10 ns and the pulse width is about 100 ns. The initial voltage of the device is 5 V, and the bombardment voltage rises by 1 V after each test. A component leakage current of greater than 1 μA indicates that the component has already failed. At this moment, the TLP will stop the ESD test.

| (a) | (b) |

Fig. 3.   (Color online) (a) Keithley-2410 and (b) TLP systems.

4. Test Results and Discussion

The test starts with the measurement of the breakdown voltage. As can be seen from Fig. 4, there are four types of device with breakdown voltages between 100 and 200 V, the other group is between 200 and 300 V, and the third group is above 300 V. Although there are some differences from the original design, it can be seen that the breakdown voltage increases with L_D. At 15 μm (S15_R), the absence of Poly2 causes the breakdown voltage to change at a rate that is not linear in relation to the HVNW change as expected. It can also be seen from the figure that the breakdown voltage of the drift-region design of the 18 μm (S18_R) sample is not markedly different from that of the 15 μm one. This is probably due to the fact that Poly2 is designed as a single turn, so the total area of Poly2 is insufficient to generate the field plate effect. This resulted in no significant increase in the breakdown voltage of the component. This phenomenon indicates that the field plate effect is very important to the breakdown voltage variation.

Then, to further analyze the ESD/latch-up capability, we used a TLP tester to measure these samples. To reduce the production and measurement errors, we measured the data of three different samples as shown in Fig. 5, which will eventually be averaged.

The test averages are arranged in Fig. 6, and the TLP IV-snapback results are shown in Fig. 6(a), where V_{t1} is the maximum triggering voltage of the parasitic BJT component and V_h is the minimum on-state voltage of the BJT. I_{t2} is the maximum current that the component can withstand. The trends of component V_{t1}–V_h are shown in Fig. 6(b). As R_{HVNW} [shown in Fig. 2(b)] increases, the parasitic BJT V_{t1} increases as the breakdown voltage of the component increases owing to the high resistance. When R_{HVNW} continues to increase, the corresponding V_{t1} and V_h of this device will also increase with it. As shown in Fig. 6(c), the increase in R_{HVNW} leads to a higher I_{t2} value owing to the relative increase in current that the device can withstand. The I_{t2} trend shows a positive relationship with L_D. Finally, the measured component breakdown voltage and TLP parameters are shown in Table 2. The FOM data in the table show that when L_D is 28 μm (S28_R), it has better I_{t2} reliability characteristics than the other devices.
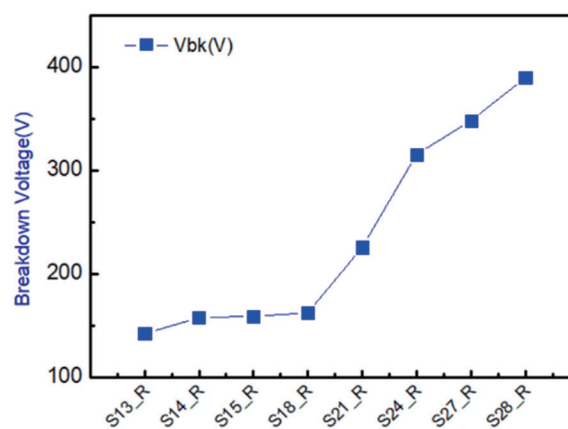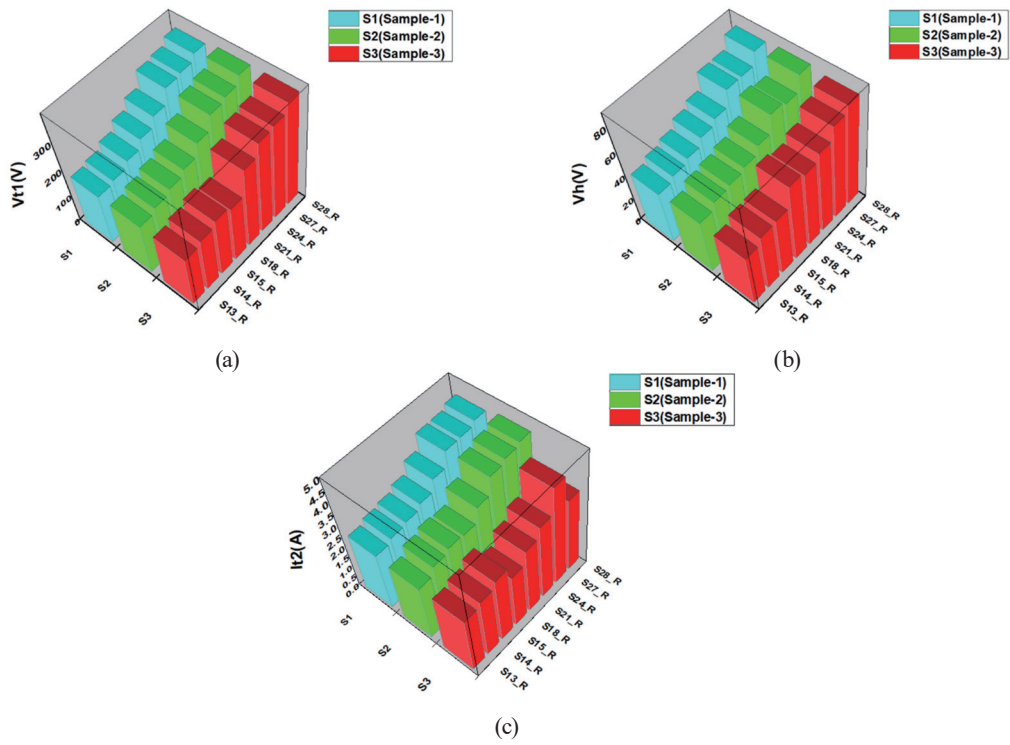

Fig. 4. (Color online) Breakdown voltage test results.

Fig. 5.　(Color online) (a) V_{t1}, (b) V_h, and (c) I_{t2} data distributions of TLP test of three different samples.
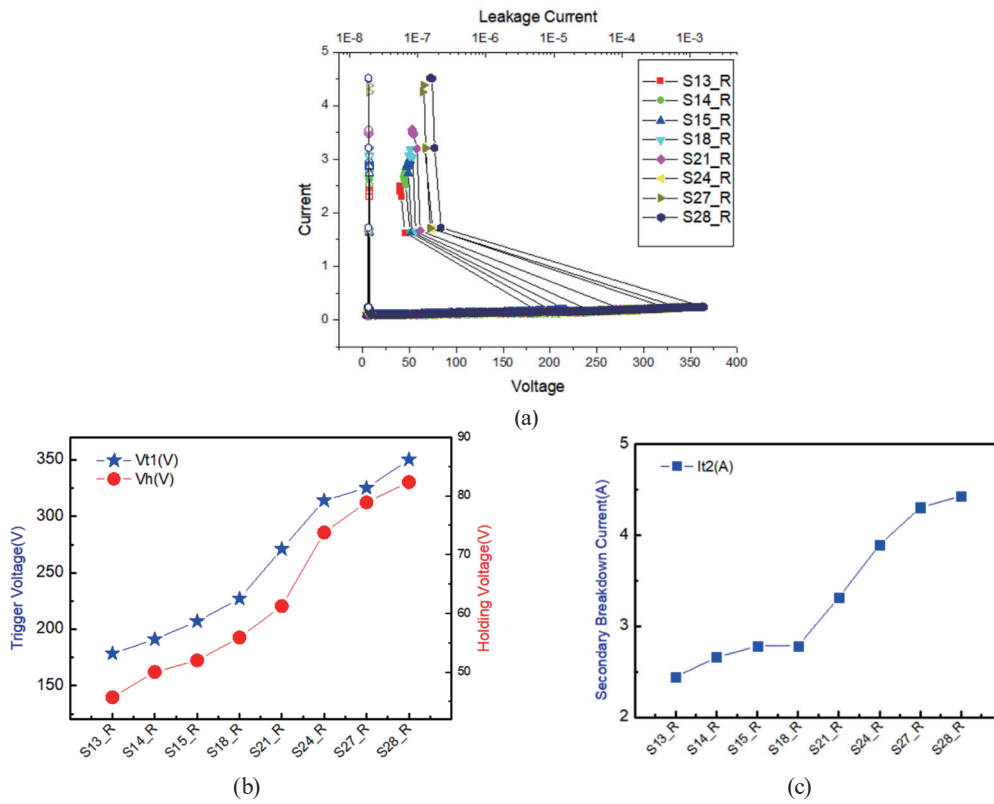

Fig. 6.　(Color online) (a) TLP snapback curves, (b) V_{t1}–V_h trend plots, and (c) I_{t2} trend plot of UHV nLDMOS-related components.

Table 2
Breakdown voltage and TLP test results of UHV nLDMOS-related components.

Cell name	V_{t1} (V)	V_h (V)	I_{t2} (A)	FOM_{TLP} (V·A/μm^2)	V_{bk} (V)
S13_R	178.39	45.77	2.44	1.70×10^2	142.71
S14_R	191.05	50.09	2.66	1.94×10^2	158.13
S15_R	207.00	52.05	2.78	2.02×10^2	159.41
S18_R	227.11	55.94	2.78	1.92×10^2	162.72
S21_R	271.06	61.29	3.31	2.24×10^2	226.05
S24_R	314.00	73.81	3.89	2.84×10^2	315.87
S27_R	325.08	78.93	4.30	3.03×10^2	348.45
S28_R	350.28	82.37	4.43	3.15×10^2	389.91

5.   Conclusions

In this paper, we focused on the modulation with a fixed gate length using the drift region to change the breakdown voltage (and operating voltage) of the components. This enables a UHV process to be used in the ultrahigh-, high-, and low-voltage ranges. The operating voltage range of a component can be adjusted by changing L_D of the component. This enables the design of ESD reliability sensors with different operating voltages. This can be seen as a change in the length of the HVNW in the drift region, which will lead to part of the curve close to a linearized high resistance. This is because the parasitic resistance R_{HVNW} varies with L_D. Finally, the FOM data show that FOM data are better than the other devices when L_D is 28 μm (S28_R). S28_R also has the highest FOM, where S28_R has an I_{t2} of 4.43 A (good ESD immunity). Compared to a device with the lowest breakdown voltage (and operating voltage) and with a drift region of 13 μm (S13_R), S28_R has an 173.22% increasing in breakdown voltage and the highest V_h (with good latch-up capability).

Acknowledgments

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