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Electrostatic Discharge Sensing of Concentric Circles of Poly2 with Different Potentials and Discrete High-voltage P-well Modulation on Circular Ultrahigh-voltage N-channel Laterally Diffused MOSFET Devices

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In this paper, we present N-channel laterally diffused MOSFET (nLDMOS) devices for electrostatic discharge (ESD) contact-mode sensors in ultrahigh voltage (UHV) applications. These circular UHV nLDMOS devices have concentric circles of poly-layer 2 (Poly2) with different potential configurations and a discrete high-voltage P-well (HVPW) in the drift region. The Poly2 on the drift region is made of polysilicon to reduce the peak electric field in the drift region, thereby reducing the on-resistance. When the Poly2 was connected to the positive VDD potential, the trigger voltage of the device decreased due to the change in the interface electric field in the drift region; thus, this device more easily triggered conduction than the Poly2 grounded type. We used five radial methods to insert the HVPW into the drift region and evenly distributed it into two, four, eight, 16, and 32 equal partitions. When the Poly2 was grounded and the HVPW layer of the drift region was divided into 32 partitions, it had the highest secondary breakdown current of 3.56 A. This is because the more uniform the distribution of the superjunction (SJ), the higher the ability of the component to discharge the ESD current. Therefore, changing the potential of Poly2 changes the electric field distribution and affects the trigger voltage. Adding an HVPW SJ structure in the drift region will increase the on-resistance, thus improving the discharging current capability.

1. Introduction

In recent years, with the advancement of semiconductor process technology, the production of electronic components has incorporated many factors such as manufacturing cost and computing speed. Despite the economic benefits of component miniaturization, it has also

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introduced many reliability problems. The electrostatic damage from the external environment is not reduced by reducing the cell area, meaning that a sensing nLDMOS device must have stronger protection to resist external ESD damage. Ultrahigh voltage (UHV) electrostatic discharge (ESD) devices are often used for the self-protection of AC-to-DC circuits and switching and lighting circuits to prevent the power IC circuits from being damage by ESD.

This paper proposes the layout design of a circular UHV nLDMOS in which concentric circles of poly-layer 2 (Poly2) are connected to different potentials and the drift region is discretely modulated to study its ESD capability. It is found that connecting the concentric circles of Poly2 with different potentials can change the electric field distribution and that high-voltage P-well (HVPW) superjunction (SJ) layers inserted in the drift region can improve the ESD capability.[1–3]

2. Layout Design of UHV Circular nLDMOS Components

2.1 Circular UHV nLDMOS reference device

We fabricated UHV nLDMOSs using a TSMC 0.5 µm UHV bipolar-CMOS-DMOS (BCD) process with the gate grounded to measure each device's immunity to ESD.[4–11] Figure 1 shows the Poly2 floating potential structure of the UHV circular nLDMOS reference device. The Poly2 on the drift region is made of polysilicon to reduce the peak electric field in the drift region, thereby reducing the on-resistance. The device has a channel length (L) of 4 µm, a total channel width (W_{tot}) of 371.96 µm, a cell area of 13396 µm^2, and an operating voltage of 200 V.

2.2 Circular UHV nLDMOS reference devices with Poly2 biased to different potentials

Figures 2(a) and 2(b) show the reference structures of the UHV circular nLDMOS with concentric circles of Poly2 connected to the positive VDD and grounded potentials, respectively. We use the field plate effect to adjust Poly2 to two different potentials, thereby changing the surface electric field in the drift region. Through this modulation, the effect of trigger and holding voltages connected to different potentials on ESD protection devices is investigated.

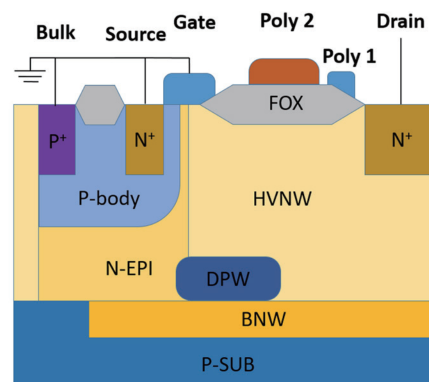

Fig. 1. (Color online) Structure of the UHV circular nLDMOS reference device with floating Poly2.

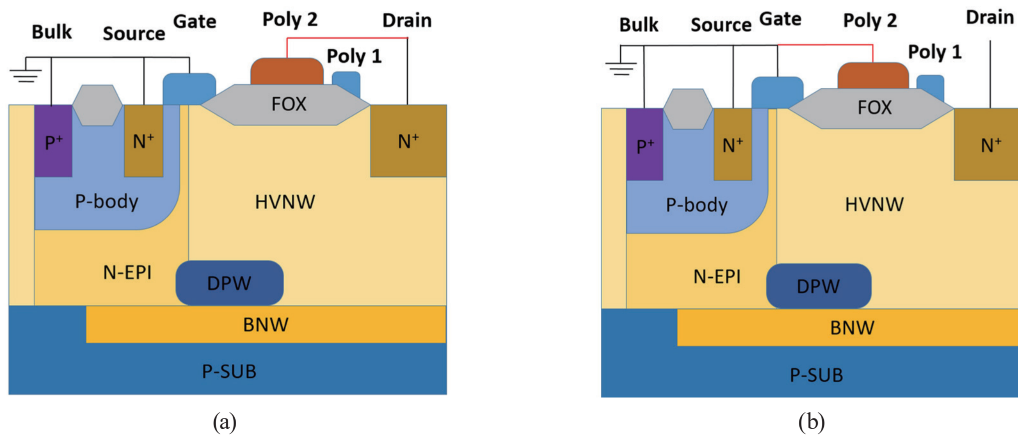

Fig. 2. (Color online) Structures of UHV circular nLDMOS reference device with Poly2 connected to (a) VDD potential and (b) VSS potential.

2.3 UHV circular nLDMOSs with Poly2 connected to positive VDD potential and discrete HVPW in drift region

Figures 3(a) and 3(b) respectively show the structure and a layout view of the UHV circular nLDMOS with Poly2 connected to the positive VDD potential and discrete HVPW modulation in the drift region. Immediately after Metal 1 is connected to the drain terminal, the concentric circles of Poly2 have a high VDD potential, and the HVPW layer is added to the drift region, which is divided into two, four, eight, 16, or 32 partitions. Figure 3(c) shows a schematic diagram of these five radial discrete layouts. The high-voltage N-well (HVNW) and HVPW are staggered to form an SJ structure.[12–14] The depletion regions formed by these PN junctions reduce the surface electric field in the drift region of the device to improve its withstand voltage and discharge current capability.

2.4 UHV circular nLDMOSs with Poly2 connected to ground and discrete HVPW modulation in drift region

Figures 4(a) and 4(b) respectively show the structure and a layout view of the UHV circular nLDMOS with Poly2 connected to the ground and discrete HVPW modulation in the drift region. Metal 1 in Fig. 4(b) is used to connect the concentric circles of Poly2 to the gate terminal and ground. Furthermore, the method used for HVPW radial modulation is discrete as shown in Fig. 3(c), but it is hidden in Fig. 4(b).

3. Experimental Results and Discussion

3.1 Testing instruments

We used a transmission line pulse (TLP) system to measure the designed components.[15] This TLP tester provides a 100-ns-wide continuous step pulse with rise and fall times of less

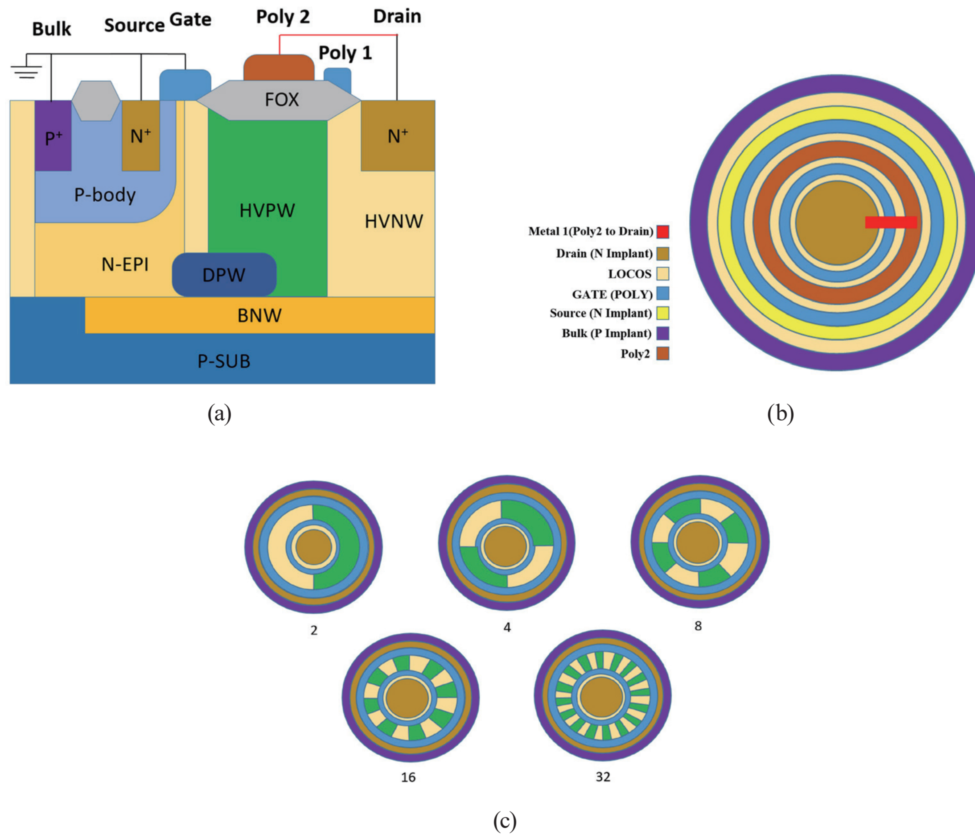

Fig. 3. (Color online) (a) Cross section, (b) layout view, and (c) HVPW radially discrete distribution in drift region of the UHV circular nLDMOS with Poly2 connected to the VDD potential.

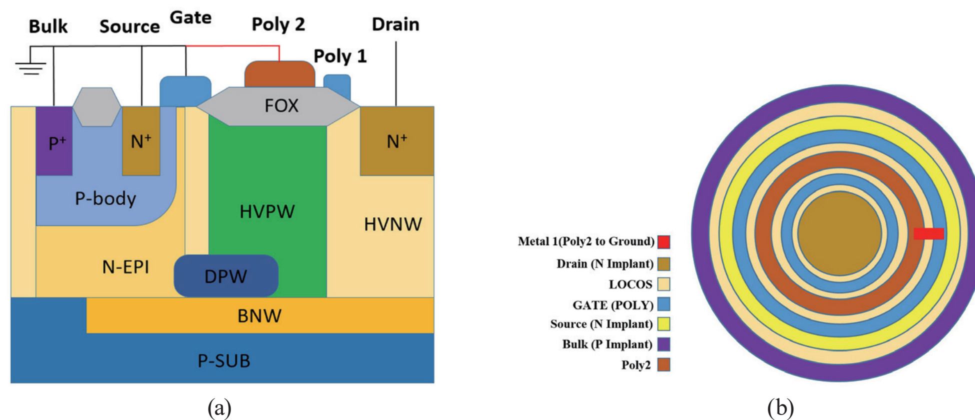

Fig. 4. (Color online) (a) Cross section and (b) layout view of UHV circular nLDMOS with Poly2 connected to ground potential and discrete HVPW modulation in drift direction.

than 10 ns. The starting voltage was 5 V, which was increased in steps of 1 V during the test. When a device under test is measured using the TLP system, if the leakage current of the component exceeds 1 μA, the measurement is stopped and the component is judged to have

failed. Then through the LabVIEW program, we captured the relationship between the voltage and current waveforms, and finally, the *I–V* snapback characteristic curve was obtained. Therefore, the important testing parameters such as trigger voltage (V_{t1}), holding voltage (V_h), on-resistance (R_{on}), and secondary breakdown current (I_{t2}) were obtained from the characteristic curve.

3.2 UHV circular nLDMOSs with Poly2 connected to different potentials

Figure 5(a) shows the TLP snapback *I–V* curves of Poly2 connected to different potentials. As shown in Fig. 5(b), compared with the Poly2 floating potential reference device, it was found that the trigger voltages of the devices connected to the VDD potential and the ground were reduced (to 266 and 284 V, respectively). Because of the change in the electric potential, the electric field distribution in the drift region of the device was changed, significantly decreasing the trigger voltage. At the same time, the holding voltage of the devices also decreased slightly. It was also found from Fig. 5(c) that the secondary breakdown current slightly decreased when the Poly2 potentials changed, which means that these potentials did not enhance the discharge capability of the ESD current.

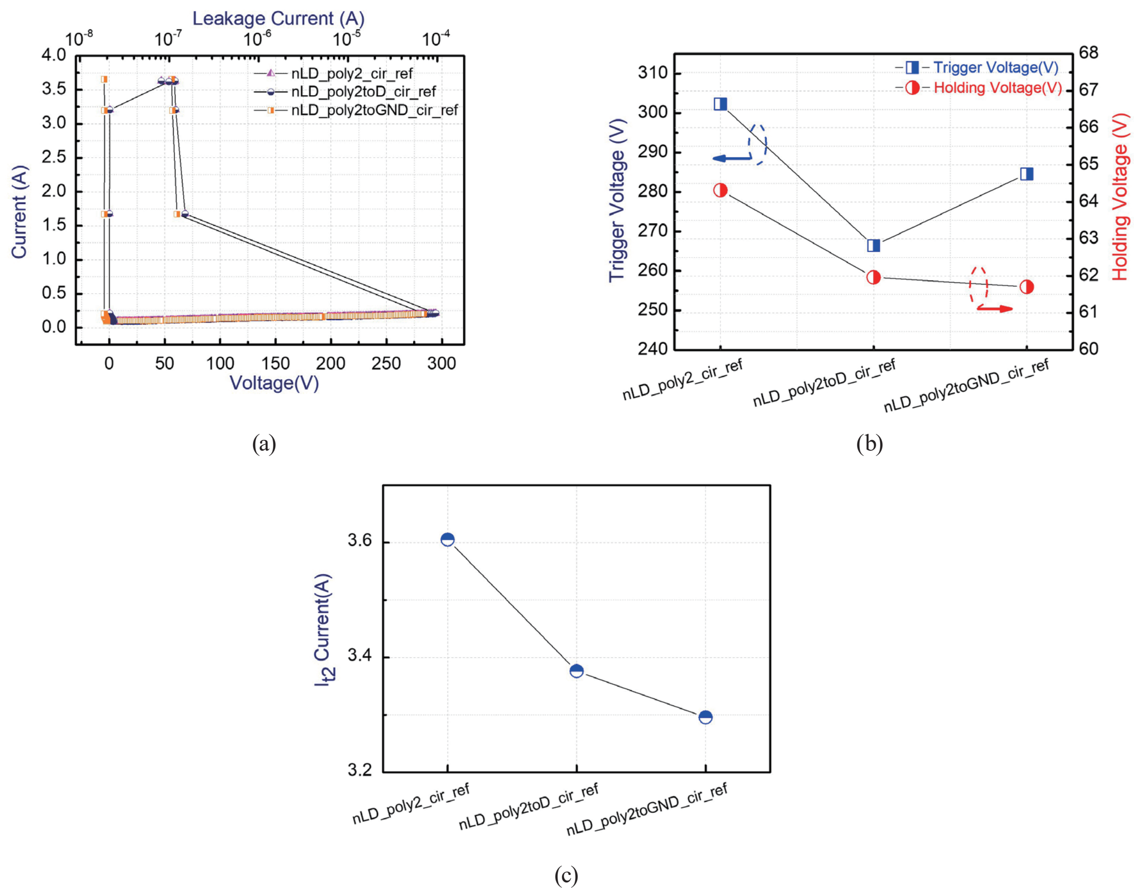

Fig. 5. (Color online) (a) TLP snapback *I–V* curves, (b) V_{t1}–V_h plot, and (c) secondary breakdown current data of UHV circular nLDMOSs with the Poly2 connected to different potentials.

3.3 UHV circular nLDMOSs with Poly2 connected to positive VDD potential with discrete HVPW modulation in drift region

The Poly2 was connected to a positive VDD potential with discrete HVPW modulation in the drift region of the UHV circular nLDMOS devices, and snapback *I–V* curves were measured using a TLP tester. The curves are shown in Fig. 6(a), where the reference device that connects the Poly2 to the positive VDD is denoted nLD_poly2toD_cir_ref. Figures 6(b) and 6(c) show that the discrete HVPW components nLD_poly2toD_cir_4 and nLD_poly2toD_cir_32 have a higher trigger voltage and secondary breakdown current than the reference device. Because discrete HVPW modulation in the drift region increased the on-resistance, the trigger voltage increased, but the difference in the secondary breakdown current was small. The measurement results and physical parameters are listed in Table 1. Among them is the figure of merit (FOM) [Eq. (1)] when the internal parasitic bipolar junction transistor (BJT) of protection component was turned on, so that ESD current can be discharged through this parasitic BJT. The FOM is the holding voltage multiplied by the maximum current per unit area of the device,

$$FOM = V_h\,(\mathrm{V}) \times I_{t2}\,(\mathrm{A}) \,/\, Cell\ Area\ (\mu\mathrm{m}^2), \tag{1}$$

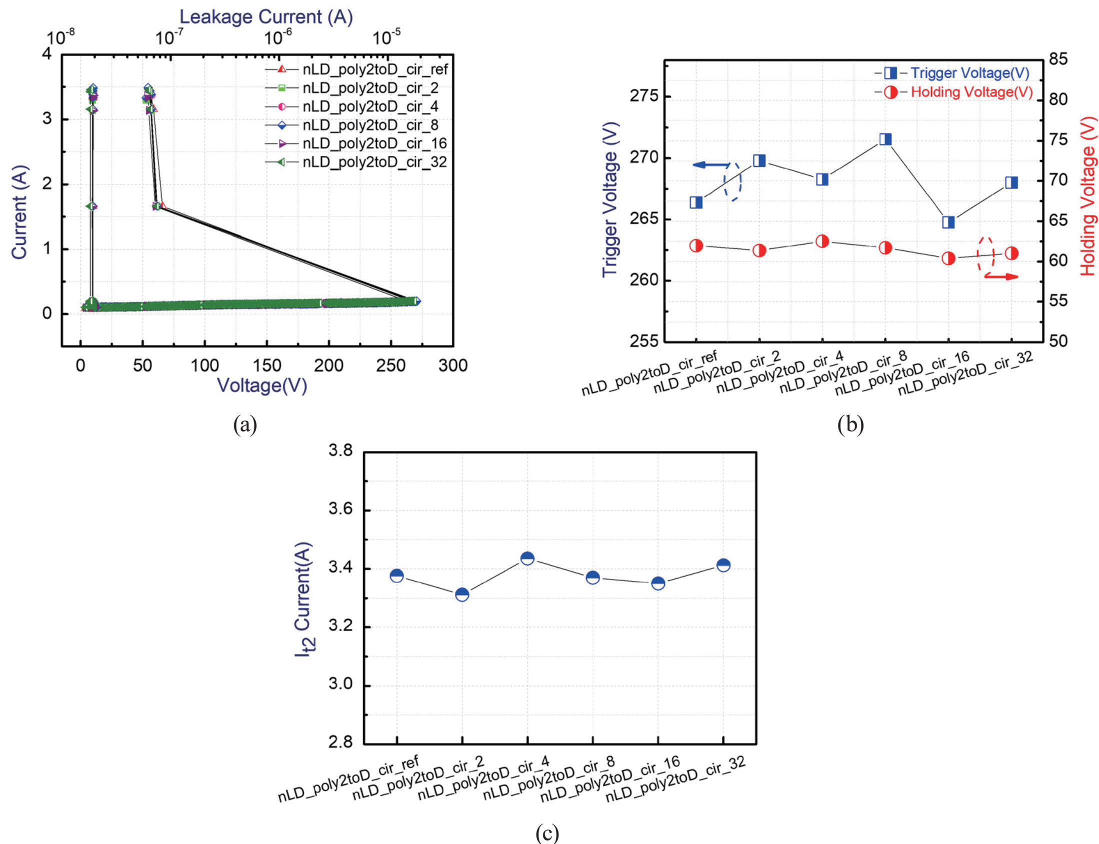

Fig. 6. (Color online) (a) TLP snapback *I–V* curves, (b) V_{t1}–V_h plot, and (c) secondary breakdown current data of UHV circular nLDMOS with the Poly2 connected to a positive VDD potential with discrete HVPW modulation in the drift region.

Table 1
Snapback characteristic parameters of UHV circular nLDMOSs with the Poly2 connected to a positive VDD potential and discrete HVPW modulation in the drift region.

nLDMOS sample	V_{t1} (V)	V_h (V)	I_{t2} (A)	FOM (V·μA/μm^2)
nLD_poly2toD_cir_ref	266.38	61.96	3.38	15616.54
nLD_poly2toD_cir_2	269.80	61.36	3.31	15168.34
nLD_poly2toD_cir_4	268.26	62.52	3.44	16032.21
nLD_poly2toD_cir_8	271.53	61.71	3.37	15523.52
nLD_poly2toD_cir_16	264.76	60.39	3.35	15101.56
nLD_poly2toD_cir_32	268.00	61.01	3.41	15541.19

where V_h is the holding voltage, I_{t2} is the secondary breakdown current, and *Cell Area* is the component cell area.

3.4 UHV circular nLDMOSs with Poly2 connected to ground and discrete HVPW modulation in drift region

The reference device that connects the Poly2 to the ground is denoted nLD_poly2toGND_cir_ref. Because the Poly2 is grounded, a grounded field plate was applied to suppress the surface electric field of the channel; thus, the trigger voltage was higher than the reference device of the Poly2 sample connected to a positive VDD potential. Figure 7(a) shows measured

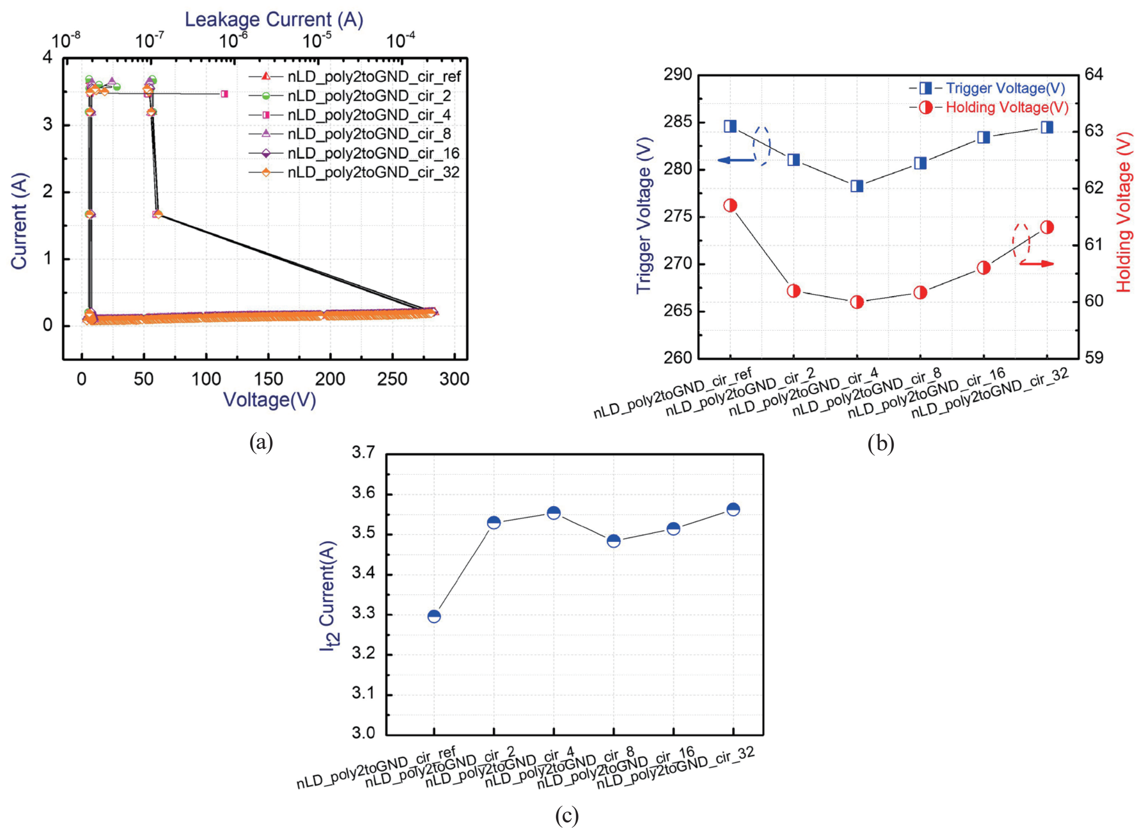

Fig. 7. (Color online) (a) TLP snapback I–V curves, (b) V_{t1}–V_h plot, and (c) secondary breakdown current data of UHV circular nLDMOSs with the Poly2 connected to the ground and discrete HVPW modulation in the drift region.

Table 2
Snapback characteristic parameters of UHV circular nLDMOSs with the Poly2 connected to the ground and discrete HVPW modulation in the drift region.

nLDMOS sample	V_{t1} (V)	V_h (V)	I_{t2} (A)	FOM (V·µA/µm^2)
nLD_poly2toGND_cir_ref	284.59	61.70	3.30	15180.72
nLD_poly2toGND_cir_2	281.04	60.20	3.53	15860.49
nLD_poly2toGND_cir_4	278.25	60.00	3.55	15918.25
nLD_poly2toGND_cir_8	280.68	60.17	3.48	15647.16
nLD_poly2toGND_cir_16	283.43	60.61	3.51	15899.99
nLD_poly2toGND_cir_32	284.47	61.32	3.56	16307.44

TLP snapback *I–V* curves of the UHV circular nLDMOSs with the Poly2 grounded and discrete HVPW modulation in the drift region. Figure 7(b) shows a comparison of the trigger voltage and holding voltage. The curves of the SJ partition of the first three groups (i.e., two, four, and eight partitions) are very similar because the current flowed through the buried N-well (BNW) layer below the HVPW when the partition number of the HVPW was small. The more discrete the HVPW, the more evenly current can flow through the HVNW, causing the trigger voltage and holding voltage to gradually increase. From the physical parameters in Fig. 7(c) and Table 2, it was found that nLD_poly2toGND_cir_32, with 32 partitions in the drift region, had the highest secondary breakdown current (I_{t2}). The more discrete the partitions of the HVPW, the higher the SJ and the more uniform the distribution. Thus, this component had the strongest discharge current capability.

3.5 Comparison and discussion

On the basis of the results in Tables 1 and 2 obtained from the previous two modulations, the trend of the FOM plots is shown in Fig. 8. From the Poly2 connected to the VDD potential, it was found that the FOM of 16032.21 V·µA/µm^2 for the HVPW with discrete modulation into four equal partitions was higher than that of the reference component (15616.54 V·µA/µm^2). Moreover, the Poly2 connected to the ground with the HVPW discretely divided into 32 equal

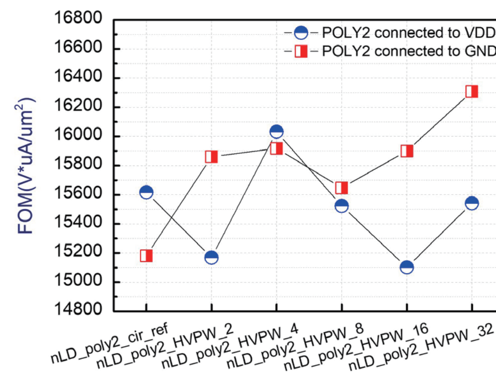

Fig. 8. (Color online) FOM trend of UHV circular nLDMOSs with the Poly2 connected to the VDD potential and ground potential with discrete HVPW modulation in the drift region.

partitions had the highest FOM of 16307.44 V·μA/μm^2. This is a significant improvement compared with the value of 15180.72 V·μA/μm^2 for the reference component (nLD_poly2toGND_cir_ref), because in the case of 32 equal partitions, the ESD current was evenly dispersed throughout the HVNW, resulting in the highest I_{t2} and the greatest discharge of ESD current.

4. Conclusions

In this paper, we proposed novel UHV ESD current sensing devices that use UHV circular nLDMOSs with concentric circles of Poly2 connected to different potentials and discrete HVPW modulation in the drift region. It was found that the trigger voltage changed when the Poly2 was connected to different potentials. Because the voltage applied to the Poly2 changed the surface electric field distribution of the nLDMOS interface, the device more easily conducted current than when the Poly2 was grounded. The maximum secondary breakdown current when the Poly2 was grounded was 3.56 A, and it was found that the device had the greatest discharge current capacity when the HVPW was divided into 32 equal partitions because the distribution of the SJ was the most uniform. It was concluded that changing the potential of the Poly2 changed the electric field distribution of the drain terminal, which decreased the trigger voltage. Moreover, the radial dispersion of the HVPW in the drift region (SJ structure) improved the ESD current discharge capability, making the proposed ESD current sensing device very suitable for applications under UHV.

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References

1 Z. Chen, A. Salman, G. Mathur, and G. Boselli: Proc. 2015 37th Electrical Overstress/Electrostatic Discharge Symp. (EOS/ESD, 2015) 1–6. https://doi.org/10.1109/EOSESD.2015.7314735
2 C. Wu, J. Lee, and C. Lien: IEEE Trans. Electron Devices **62** (2015) 4135. https://doi.org/10.1109/TED.2015.2493879
3 H. Y. Shen, S. R. Dong, Z. K. Xu, T. Hu, W. Guo, and W. Huang: Proc. 2019 IEEE 26th Int. Symp. Physical and Failure Analysis of Integrated Circuits (IPFA, 2019) 1–4. https://doi.org/10.1109/IPFA47161.2019.8984830
4 J. Hao and D. Hahn: Proc. 2016 IEEE Int. Integrated Reliability Workshop (IIRW, 2016) 41–44. https://doi.org/10.1109/IIRW.2016.7904897
5 H. Cha, K. Lee, J. Lee, and T. Lee: Proc. 2016 28th Int. Symp. Power Semiconductor Devices and ICs (ISPSD, 2016) 423–426. https://doi.org/10.1109/ISPSD.2016.7520868
6 Y. Chen, C. Lee, M. Tsai, C. Lee, and C. Wang: Proc. 2018 IEEE 30th Int. Symp. Power Semiconductor Devices and ICs (ISPSD, 2018) 331–334. https://doi.org/10.1109/ISPSD.2018.8393670
7 W. Chen, J. Pjencak, M. Agam, J. Janssens, R. Jerome, S. Menon, and M. Griswold: Proc. 2021 33rd Int. Symp. Power Semiconductor Devices and ICs (ISPSD, 2021) 287–290. https://doi.org/10.23919/ISPSD50666.2021.9452294
8 F. B. Du, S. Y. Song, F. Hou, W. Q. Song, L. Chen, J. Z. Liu, Z. W. Liu, and J. J. Liou: IEEE Electron Device Lett. **40** (2019) 1491. https://doi.org/10.1109/LED.2019.2926103
9 K. I. Do, B. B. Song, and Y. S. Koo: IEEE Trans. Device Mater. Reliab. **20** (2020) 716. https://doi.org/10.1109/TDMR.2020.3022897

10 P. Mahajan, R. Kumar, R. Gauthier, and K. J. Hwang: Proc. 2020 Int. EOS/ESD Symp. Design and System (IEDS, 2020) 1−6. https://doi.org/10.23919/IEDS48938.2021.9468827
11 Y. Wang, G. Lu, and Y. Wang: IEEE Access **8** (2020) 64730. https://doi.org/10.1109/ACCESS.2020.2972042
12 J. R. Tsai, Y. M. Lee, M. C. Tsai, G. Sheu, and S. Yang: Proc. 2011 IEEE Region 10 Conf. (TENCON, 2011) 760−763. https://doi.org/10.1109/TENCON.2011.6129212
13 B. Duan, M. Li, Z. Dong, Y. Wang, and Y. Yang: IEEE Trans. Electron Devices **66** (2019) 4836. https://doi.org/10.1109/TED.2019.2939233
14 N. He, S. Zhang, X. Zhu, X. Li, H. Wang, and W. Zhang: Proc. 2020 32nd Int. Symp. Power Semiconductor Devices and ICs (ISPSD, 2020) 419−422. https://doi.org/10.1109/ISPSD46842.2020.9170046
15 Y. Lu, Y. Hong, and Y. Cheng: Proc. 2021 5th IEEE Electron Devices Technology & Manufacturing Conf. (EDTM, 2021) 1−3. https://doi.org/10.1109/EDTM50988.2021.9420937

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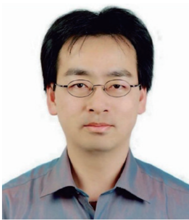

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