

Comparison of Parasitic Capacitances of Packaged Cascode Gallium Nitride Field-effect Transistors

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In this work, we examined the electrical characteristics of laboratory-fabricated cascode gallium nitride field-effect transistors (GaN FETs) and analyzed their parasitic capacitances. The calculated results were in good agreement with the experimental results and showed that commercial GaN FETs have superior switching performance, whereas laboratory-fabricated GaN FETs require further improvement.

1. Introduction

Wide-bandgap devices consisting of gallium nitride (GaN) or silicon carbide (SiC) have superior material properties that make them the most suitable candidate to replace Si-based transistors.⁽¹⁾ Since using these new power devices in GaN-based switching converter applications may be challenging, knowing the device characteristics is necessary. However, using GaN in power design fields with a high-switching condition engenders certain design challenges.⁽²⁾ To assist designers in the switching application of GaN FETs, parasitic effect issues must be addressed. In recent years, several GaN FET device models have been reported in the field of power conversion. These models were partially collated and analyzed in the literature.⁽³⁾ Among these models, the behavioral model can be developed through applying experimentally extracted parameters. To accurately evaluate switching performance, many previous studies have developed behavioral models to obtain realistic characteristic curves. Such models include a power loss estimation model;⁽⁴⁾ a simple GaN power transistor model with temperature- and frequency-dependent inductor circuits,⁽⁵⁾ which exhibited strong static characteristics; and a model considering detailed parasitic inductance and cascode capacitance.^(6,7) Other models include one with turn-off resistance that was developed for sorting device uniformity.⁽⁸⁾ The goal of all the aforementioned studies was to develop GaN FET models that are more practical than real power devices. The goal was the same for the present study. In previous studies, several laboratory-fabricated GaN FETs such as those based on flip-chip packaging and wire bonding have been proposed.^(9,10) The electrical characteristics of D-mode

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and cascode devices have also been studied.⁽¹⁰⁾ However, parasitic effects on laboratory-fabricated cascode GaN FETs have not been determined in any of the aforementioned studies. GaN-based sensors have been proposed for gas sensing, pH measurement, heavy metal detection, biotoxin sensing, and biomedical applications, owing to their promising results including fast response, small device size, and chemical and thermal stability.^(11,12) Sensors with rapid response need fast switching performance. The parasitic capacitance of a GaN FET is a significant factor in determining the switching response during the switching transition.⁽¹³⁾ The faster the gate charge is supplied, the faster the device will change the switching transition.⁽¹³⁾ The present study involved two stages. First, the device structure of metal-insulator-semiconductor high-electron-mobility transistors (MIS-HEMTs) was introduced, and static characterization was performed using a curve tracer and a capacitance–voltage (C – V) analyzer.⁽¹⁴⁾ Second, the analysis of parasitic capacitances on the fabricated cascode GaN FET model was demonstrated.

2. Materials and Methods

2.1 Device structure of MIS-HEMT

Figure 1(a) shows a simplified schematic of the fabricated AlGaN/GaN MIS-HEMT used in this study. The thicknesses of the $\text{Al}_{0.23}\text{Ga}_{0.77}\text{N}$ and GaN layers are 20 nm and 2.1 μm , respectively. The gate-to-drain spacing is 17 μm and the gate-to-source spacing is 3 μm . The gate length is 1 μm and the gate width is 1 mm. The device has 80 fingers, so the total gate width is 80 mm. The detailed device fabrication information is shown in Ref. 10. The MIS-HEMT is a normally-on device; without an applied negative gate-source voltage, the device is in the on-state. Connection to a low-voltage cascode metal-oxide-semiconductor field-effect transistor (LV MOSFET) allows normally-on MIS-HEMT devices to act as normally-off devices, as shown in Fig. 1(b). The MIS-HEMT was a 600 V, 330 m Ω device,⁽¹⁰⁾ and the LV MOSFET chosen was a 30 V OptiMOS^{TM3} with an $R_{DS(on)}$ of 3.1 m Ω .⁽¹⁵⁾ Studies have demonstrated the characteristics of laboratory-fabricated D-mode and cascode GaN FETs. Owing to variations in device fabrication, wire bonding, and packaging, device characteristics must be measured to obtain detailed device information. For comparison, commercial cascode GaN FETs are used in this study.⁽¹⁶⁾

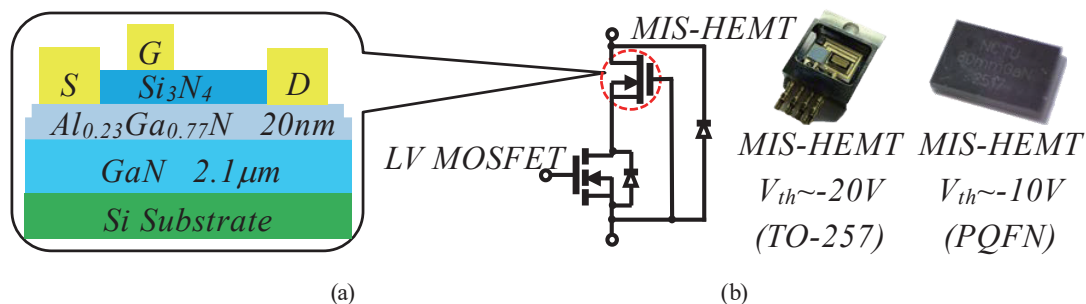


Fig. 1. (Color online) Schematic of (a) MIS-HEMT (normally-on) and (b) cascode GaN FET.

2.2 Electrical characteristics of cascode GaN FETs

The static characteristics, namely the transfer characteristics ($I_{DS}-V_{GS}$), and parasitic capacitances of cascode GaN FETs, are described in the following section. From the static characteristics, the plateau voltage (V_{PL}) in the gate charge curve can be read from the transfer characteristic graph with the test current whereas the gate charge can be derived from parasitic capacitance curves. Gate charge information can predict the switching behavior.

2.2.1 Transfer characteristics ($I_{DS}-V_{GS}$)

The transfer characteristics of the commercial GaN FET and fabricated D-mode MIS-HEMT for various V_{GS} values are tested in the range of -25 to 1 V measured at 1 V increments with a V_{DS} of 10 V, similarly to the commercial and fabricated cascode GaN FET transfer characteristics for V_{GS} values ranging from 0 to 6 V measured at 1 V increments with a V_{DS} of 10 V.

2.2.2 Parasitic capacitances (C_{gs} , C_{gd} , and C_{ds})

The parasitic capacitances C_{iss} , C_{oss} , and C_{rss} can be represented as $C_{iss} = C_{gs} + C_{gd}$, $C_{oss} = C_{gs} + C_{ds}$, and $C_{rss} = C_{gd}$, respectively. The detailed measurements of the parasitic capacitances are explained in Ref. 8. The measurements were conducted within an AC frequency range of 100 kHz– 1 MHz. C_{gs} was measured at 100 kHz, whereas C_{ds} and C_{gd} were measured at 1 MHz with an oscillation level of 30 mV.

2.2.3 Analysis of cascode parasitic capacitances

Figure 2 shows the equivalent capacitance of the cascode GaN FET structure in this study. Capacitances labeled with the subscripts “C”, “M”, “J”, and “D” represent cascode GaN FET, LV MOSFET, MIS-HEMT, and SiC Schottky barrier diode (SBD), respectively. The cascode parasitic capacitances are divided into three regions: $V_{DS_M} < |V_{P_J1}|$, $|V_{P_J1}| \leq V_{DS_M} < |V_{P_J2}|$, and $V_{DS_M} \geq |V_{P_J2}|$.

As the MOSFET drain-source voltage is smaller than the absolute value of the first MIS-HEMT pinch-off-voltage (V_{P_J1}) ($V_{DS_M} < |V_{P_J1}|$), the MIS-HEMT channel is conducting because of its normally-on characteristics. The cascode input capacitance (C_{iss_C}) is the sum of C_{gs_M} and C_{gd_M} in the LV MOSFET represented as Eq. (1). The transfer capacitance (C_{rss_C}) is the C_{gd_M} of the LV MOSFET represented as Eq. (2). The conducting channel of the MIS-HEMT connects the output capacitance of the MOSFET (C_{oss_M}) [gate–drain capacitance (C_{gd_M}) and drain–source capacitance (C_{ds_M})] in parallel with the input capacitance of the MIS-HEMT (C_{iss_J}) [gate–drain capacitance (C_{gd_J}) and gate–source capacitance (C_{gs_J})], and the output capacitance of the cascode can be represent as Eq. (3):

$$C_{iss_C,1} = C_{gs_M} + C_{gd_M}, \quad (1)$$

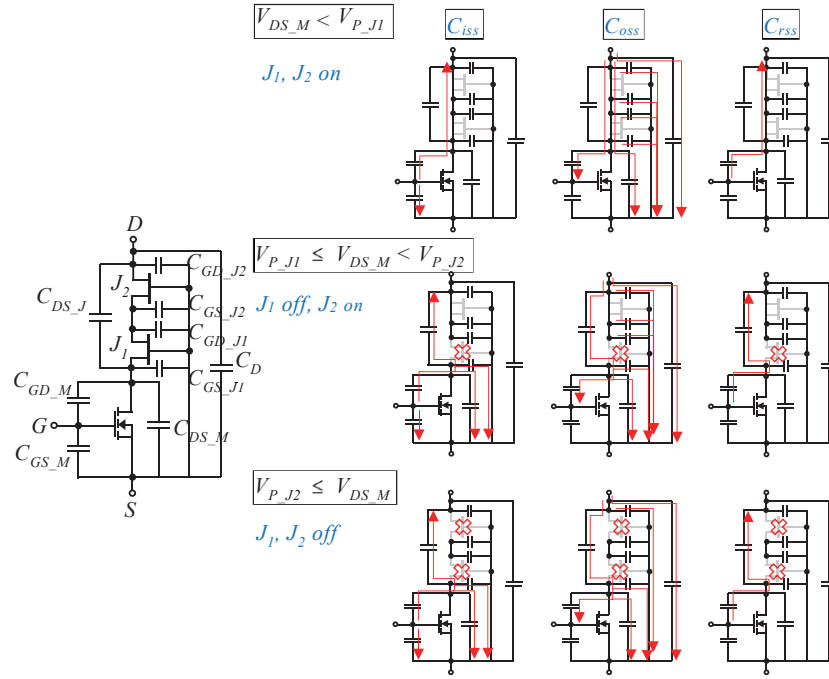


Fig. 2. (Color online) Equivalent capacitance of fabricated cascode GaN FET structure.

$$C_{rss_C,1} = C_{gd_M}, \quad (2)$$

$$C_{oss_C,1} = C_{gd_M} + C_{ds_M} + C_{gs_J1} + C_{gd_J1} + C_{gs_J2} + C_{gd_J2}. \quad (3)$$

As the drain-to-source voltage of the MOSFET (V_{ds_M}) reaches above the first pinch-off voltage of the MIS-HEMT (V_{P_J1}) and below the second pinch-off voltage of the MIS-HEMT (V_{P_J2}) ($|V_{P_J1}| \leq V_{DS_M} < |V_{P_J2}|$), the first MIS-HEMT starts to block voltage. In the second stage, the cascode input capacitance ($C_{iss_C,2}$) is the sum of C_{gs_M} and C_{gd_M} in the series of C_{ds_M} , C_{ds_J} , and C_{gs_J1} , which are in parallel with each other, represented as Eq. (4), the transfer capacitance ($C_{rss_C,2}$) is C_{gd_M} in the series of C_{ds_J} , represented as Eq. (5), and the cascode output parasitic capacitance ($C_{oss_C,2}$) is the sum of C_{gd_J1} , C_{gs_J1} , C_{gd_J2} , C_D , and C_{ds_J} in the series of C_{gd_M} , C_{ds_M} , and C_{gs_J1} , which are in parallel with each other, represented as Eq. (6):

$$C_{iss_C,2} = C_{gs_M} + \frac{C_{gd_M}(C_{ds_M} + C_{ds_J} + C_{gs_J1})}{C_{gd_M} + (C_{ds_M} + C_{ds_J} + C_{gs_J1})}, \quad (4)$$

$$C_{rss_C,2} = \frac{C_{gd_M} \cdot C_{ds_J}}{C_{gd_M} + C_{ds_J}}, \quad (5)$$

$$C_{oss_C,2} = C_{gd_J1} + C_{gs_J2} + C_{gd_J2} + C_D + \frac{C_{ds_J}(C_{gd_M} + C_{ds_M} + C_{gs_J1})}{C_{ds_J} + (C_{gd_M} + C_{ds_M} + C_{gs_J1})}. \quad (6)$$

As the drain-to-source voltage of the MOSFET (V_{ds_M}) is above the second pinch-off voltage of the MIS-HEMT (V_{P_J2}) ($V_{DS_M} \geq |V_{P_J2}|$), the second MIS-HEMT starts to block voltage. In the third stage, the cascode input capacitance ($C_{iss_C,3}$) and transfer capacitance ($C_{rss_C,3}$) are the same as the cascode input capacitance ($C_{iss_C,2}$) and transfer capacitance ($C_{rss_C,2}$) in the second stage represented as Eq. (4) and Eq. (5), whereas the cascode output parasitic capacitance ($C_{oss_C,3}$) is the sum of C_{gd_J2} , C_D , and C_{ds_J} in the series of C_{gd_M} , C_{ds_M} , and C_{gs_J1} , which are in parallel with each other, represented as Eq. (7):

$$C_{oss_C,3} = C_{gd_J2} + C_D + \frac{C_{ds_J}(C_{gd_M} + C_{ds_M} + C_{gs_J1})}{C_{ds_J} + (C_{gd_M} + C_{ds_M} + C_{gs_J1})}. \quad (7)$$

2.2.4 Gate charge curve (V_{GS} - Q_{GS})

The test fixture employed for measuring the gate charge curve, which can be taken from the oscilloscope, is illustrated in Ref. 17. A plot of gate-to-source voltage versus time measured on the oscilloscope can be converted to a plot of gate-to-source voltage versus gate charge because of the relationship $Q_G = I_G \times t$. In the test, the drain-source voltage V_{DD} was set to 100 V and the load resistance R_L to 10 Ω . The load current I_D was set to 10 A because the turn-on resistance $R_{DS(on)}$ of the test device was low. The constant gate current I_g was set to approximately 1 mA by using a supply voltage of $V_{CC} = 10$ V, a pnp bipolar junction transistor (BJT), a 3.3 V Zener diode (V_{ZD}), and two resistors, 2.7 k Ω (R_E) and 10 k Ω (R_S).

3. Results

The red triangles and blue circles in the figure represent the plots for I_{DS} versus V_{GS} for the fabricated D-mode and cascode devices, respectively, as shown in Fig. 3. The threshold voltage was determined according to the intersection between the tangent and horizontal axis. The threshold voltage of the fabricated D-mode MIS-HEMT was -20 V, whereas that of the cascode device was 1.9 V. The threshold voltage of the commercial GaN FET was about 3 V.

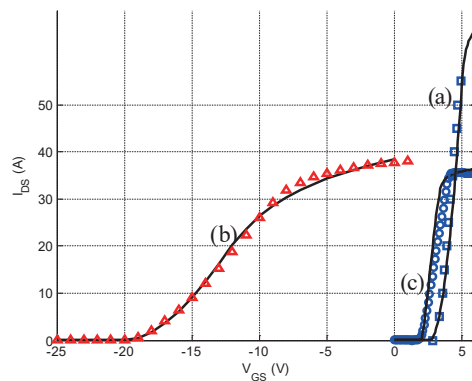


Fig. 3. (Color online) Transfer characteristics of (a) commercial (blue rectangle) and (b) fabricated MIS-HEMT (red triangle), and (c) cascode (blue circle) GaN FETs (the solid line shows the SPICE simulation).

Figure 4 illustrates the parasitic capacitances of the fabricated D-mode MIS-HEMT and cascode GaN FETs. In the D-mode MIS-HEMT, the input capacitance C_{iss} , output capacitance C_{oss} , and reverse transfer capacitance C_{rss} at $V_{GS} = -25$ V ($V_G = 0$, $V_S = 25$ V) and $V_D = 125$ V (relative drain-to-source voltage $V_{DS} = 100$ V) were 56, 50.6, and 8.64 pF, respectively. The corresponding values in the cascode GaN FET at $V_{GS} = 0$ V and $V_{DS} = 0$ V were 4350, 5250, and 505 pF; and those at $V_{GS} = 0$ V and $V_{DS} = 100$ V were 4350, 110, and 1.84 pF. The parasitic capacitances of the cascode GaN FET were higher than those of the D-mode MIS-HEMT because of the parasitic capacitance of the cascode LV MOSFET. The input capacitance (C_{iss}) and output capacitance (C_{oss}) of the fabricated GaN FET were approximately one order higher than those of the commercial GaN FET, whereas the transfer capacitance (C_{rss}) values of the two devices were the same when the V_{DS} biasing voltage was above 20 V. V_J and M were extracted through curve fitting with numerical analysis software (MATLAB) from the measured $C-V$ characteristics of the device. The commercial cascode capacitance considerably decreased at 22 V [Fig. 4(a)], whereas the fabricated cascode capacitance decreased abruptly at 20 V [Fig. 4(b)], which is exactly the threshold voltage $V_{TH\text{GaN}}$ of the GaN FETs. The V_{TH} values of the first and second junction field-effect transistors (JFETs) for commercial GaN FETs were chosen as 21 and 22 V, whereas those for the fabricated GaN FETs were chosen as 19 and 20 V, respectively. After the parasitic capacitances have been created, the simulation can be applied to obtain the created parasitic capacitances of the transistors by following the steps in Ref. 18. The measurement and simulation exhibited excellent agreement.

Because the constant current of 1 mA is charged into the gate, each division of the horizontal axis can be read in nanocoulombs when the time scale is expressed in microseconds. Figure 5 illustrates the gate charge waveforms of the commercial and fabricated cascode GaN FETs. Figure 6(a) shows the measured parasitic capacitance. The laboratory-fabricated cascode GaN FET (TO-257) has the largest input parasitic capacitance (C_{iss}) compared with the commercial cascode GaN FET and CoolMOS. The laboratory-fabricated cascode GaN FET with different

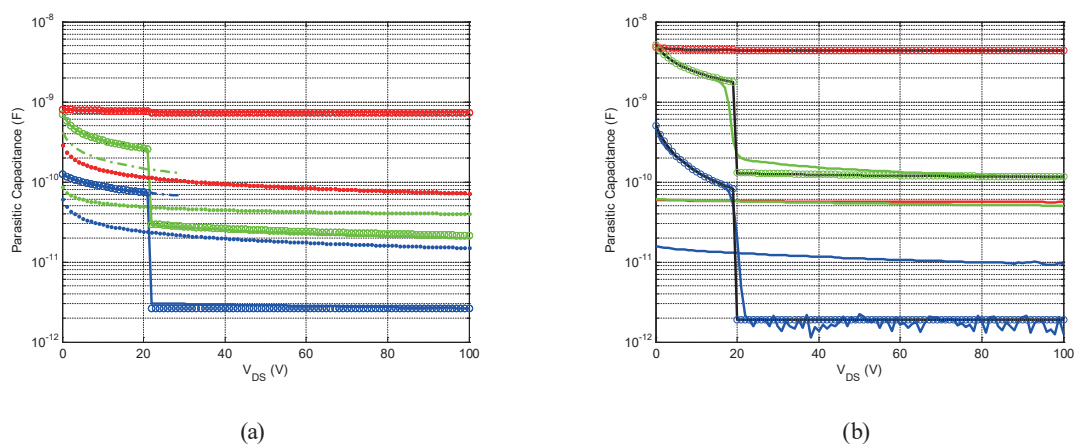


Fig. 4. (Color online) Parasitic capacitances of (a) commercial and (b) fabricated GaN FETs (dotted line, measured; black solid line, simulation; circle, calculated).

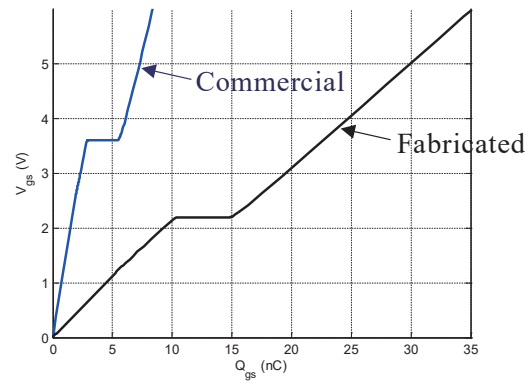


Fig. 5. (Color online) Gate-to-source voltage (V_{GS}) vs total gate charge (Q_G).

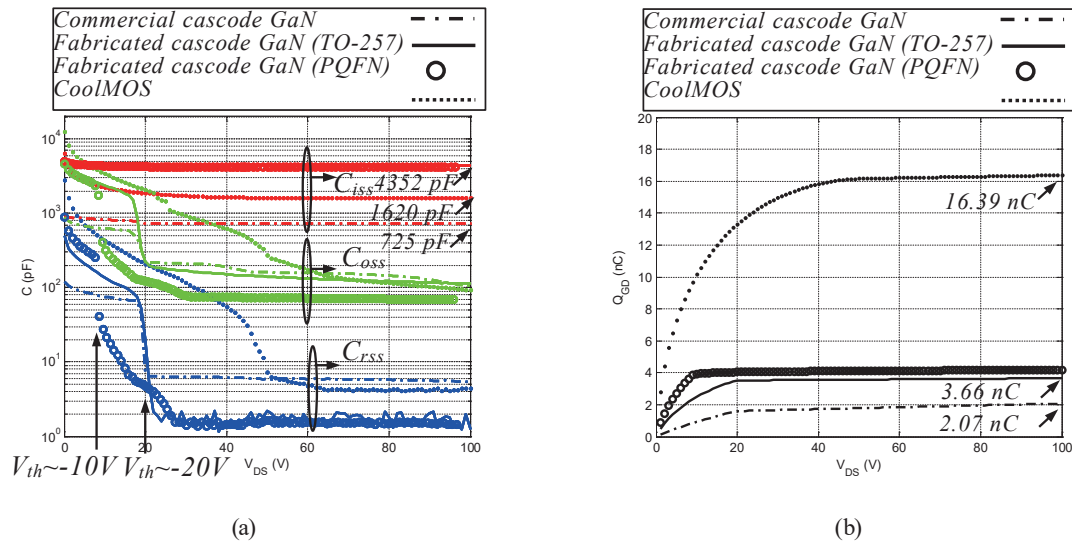


Fig. 6. (Color online) Comparison of (a) measured parasitic capacitance and (b) measured Miller charge (Q_{GD}).

threshold voltage (~ -10 V) and power quad flat no lead (PQFN) package also faces the large input parasitic capacitance problem because it has the same cascode LV MOSFET. The input parasitic capacitance of the cascode LV MOSFET dominates; therefore, the optimal LV MOSFET should be chosen. Nevertheless, it is still better than the CoolMOS when considering the Q_{GD} charge. Figure 6(b) shows the Miller charge (Q_{GD}) values of the fabricated cascode GaN FET, commercial cascode GaN FET, and CoolMOS.⁽¹⁹⁾ The Q_{GD} charge of the fabricated cascode GaN FET (3.66 nC) is higher than those of the commercial cascode GaN FET (2.07 nC), but lower than those of CoolMOS (16.39 nC). A lower Q_{GS} means that the switching drain-to-source current waveform has a shorter current transition period, and a lower Miller charge shows that the switching drain-to-source voltage waveform has a shorter voltage transition period. The lower the charge required, the shorter the transition will take, and the lower the switching losses.^(13,20)

4. Conclusions

In this study, we examined GaN FET electrical characteristics using $C-V$ plot, gate charge curve, and their switching performance. We also analyzed the cascode GaN FET capacitance. GaN FETs with lower parasitic capacitance have lower gate charge requirements, enabling faster switching. The laboratory-fabricated cascode GaN FET has the largest input parasitic capacitance (C_{iss}); thus, we should choose an optimal LV MOSFET to improve the switching performance.

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